Report No. 187

GRAPHICAL PROCESSING USING HYBRID ANALOG-DIGITAL CIRCUITRY

by

David P. Casasent

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DEPARTMENT OF COMPUTER SCIENCE · UNIVERSITY OF ILLINOIS · URBANA, ILLINOIS

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1. INTRODUCTION

1.1 Paramatrix System

The Paramatrix system of pattern representation and manipulation, proposed by W. J. Poppelbaum, employs hybrid analog-digital circuits to represent and manipulate (i.e., translate, rotate, magnify) a line drawing.

This line drawing is displayed on a two-dimensional grid of lights which is called a "matrix." The feed-system of the lights is composed of 32 parallel X lines and 32 parallel Y lines, thus creating 1024 points of intersection. Each X and Y line is referred to by some reference voltage level to enable transformation of points to be done by conventional analog methods.

The graph of X versus F(X) is referred to as the input pattern. It is set on potentiometers. If $F(X_i)$ is V volts, then the matrix intersection (X_i, Y_j) where Y_j = V volts, the analog level of line Y_j, is illuminated by means of a flipflop which drives a light bulb placed at the intersection.

Obviously to illuminate more than one light bulb in a given row, more than one F(X) versus X graph must be provided.

1.2 Transformer

Once the F(X) versus X graphs are set and the line drawing has been displayed by the matrix array of light bulbs, it may be desirable to transform this line drawing by any or all of the following transformations: translation, rotation, magnification. The device which performs these operations is called the transformer.

Various limits have been fixed on the above three operations. Translation up or down and left or right by as many as 32 steps, rotation about the geometric center of the matrix by an angle θ, $0^\circ \leq \theta \leq 360^\circ$, and

magnification by m in the X direction and n in the Y direction where m does not have to equal n, $\frac{1}{4} \leq m,n \leq 4$, must be made available. These operations must be done at a speed of about 100 kc and with an accuracy of one per cent.

The 32 X coordinates have been assigned voltages $-7.5 \leq X_i \leq 8.0$ volts. Thus the voltage by which X_i is designated differs from that of X_{i+1} by 0.500 volts. The Y coordinates are similarly designated.

1.3 The Equations of Transformation

The voltages which designate the X and Y coordinates under investigation were chosen so that they would be symmetric about the center of the matrix. This makes the operation of magnification one of simply multiplying each X and Y coordinate value by the magnification factor desired. This, however, implies that the line drawing to be magnified be centered at the (0.0 volt, 0.0 volt) matrix point which shall be designated the origin. This was found to be the best method of magnification despite this limitation.

Similarly, rotation occurs about the matrix origin and this implies that the geometric center of the figure lie at the matrix origin. Since this is necessary anyway for magnification, this restriction is very minor.

In transforming a figure the following order is the one which will yield the desired results most easily:

(1) Translation of the figure until the geometric center lies at the matrix origin,

(2) Magnification, and

(3) Rotation.

Designating the initial coordinates of the figure as x, y and the transformed coordinates as X, Y, the transformation equation is

$$(X,Y) = RMT(x,y). \qquad (1.1)$$

Defining a as the amount of translation in the X direction, b as the amount of translation in the Y direction, θ as the angle of rotation, m as the magnification factor in the X direction, and n as the magnification factor in the Y direction, the equations of transformation become:

$$X = m(x + a) \cos \theta + n(y + b) \sin \theta \qquad (1.2)$$

$$Y = -m(x + a) \sin \theta + n(y + b) \cos \theta \ . \qquad (1.3)$$

The transformer, however, inspects each of the 1024 matrix points (X_i, Y_j), i, j = 0 ... 31 and determines what initial matrix point with the given values of a, b, θ, m, and n would have generated the point in question. In other words, the inputs to the transformer are X and Y, the output or transformed coordinates, and the outputs are x and y, the initial coordinates.

There will be 1024 pairs of inputs, one for each of the 1024 matrix points. For each of these the transformer will generate a corresponding pair of input coordinates (x_{ij}, y_{ij}) which, under the transformation chosen, would yield the output coordinates (X_i, Y_j) which are being investigated. Depending on whether the generated matrix intersection (x_{ij}, y_{ij}) was activated on the initial figure, the corresponding transformed point (X_i, Y_j) will be activated or left alone. The following intersection (X_i, Y_{j+1}) is then similarly inspected and the process continues until the entire matrix grid has been scanned.

This method of transformation is the simplest to implement in hardware.

The transformation equations that the transformer solves correspond to performing the inverse operations done on the matrix and in the opposite order. The order of the operations that the transformer performs is rotation, demagnification, and translation. Rotation and translation are performed with the opposite sign conventions as before. The actual equations of transformation take the following form:

$$x_{ij} = \frac{1}{m} [X_i \cos \theta - Y_j \sin \theta] - a \qquad (1.4)$$

$$y_{ij} = \frac{1}{n} [X_i \sin \theta + Y_j \cos \theta] - b \qquad (1.5)$$

$$i, j = 0 \ldots 31$$

where X_i and Y_j assume all 1024 possible combinations of 32 X and 32 Y coordinates.

Theoretically, the order for the operations of magnification and rotation is unimportant since both require only that the center of the figure lie at the matrix origin. Obviously, translation must be performed first on the matrix. If the order of magnification and rotation were not chosen as in equations (1.2) and (1.3) then the common factors 1/m and 1/n would not occur in equations (1.4) and (1.5) and the equations of transformation would be more difficult to generate.

It is quite possible that in the generation of the equations of transformation certain coordinate voltage levels after magnification and translation could reach quite high values. The circuits of the transformer are designed so that such voltages will be set to +10 volts or -10 volts.

1.4 Block Diagram of the Paramatrix System

Figure 1 contains a block diagram of the Paramatrix system.

This paper will be concerned only with the transformer portion of the Paramatrix system together with part of its peripheral equipment necessary to generate the equations of transformation. The major emphasis will be on an ultralinear voltage amplifier (Section 5).

Further information and discussion regarding the other portions of this system can be found in the various DCS Technical Progress Reports listed in the Bibliography.

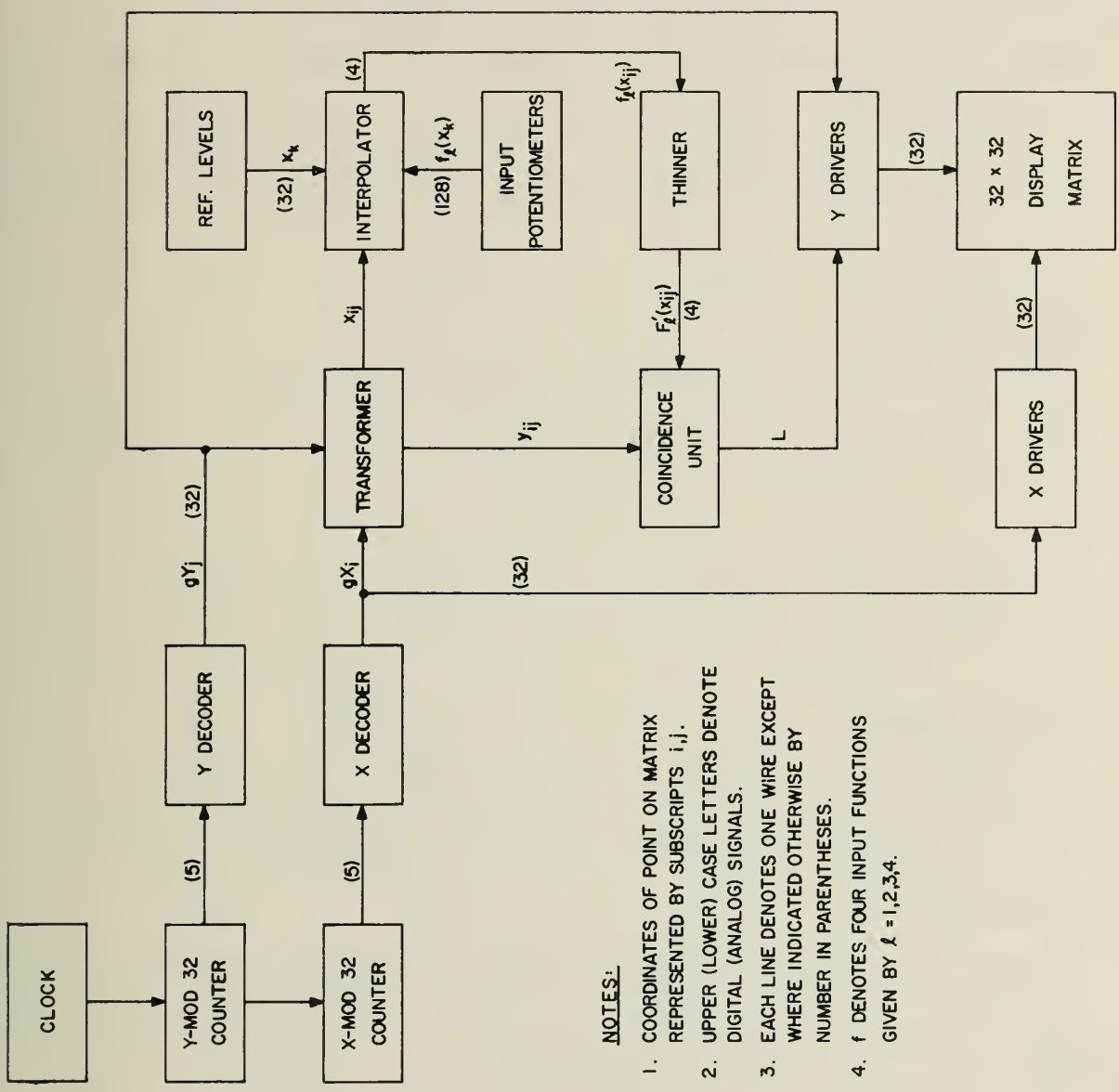


Figure 1. Block Diagram of Paramatrix System.

2. GENERATION OF X_i AND Y_j

2.1 X and Y Counter

The X and Y matrix coordinates have been designated $X_0 \ldots X_{31}$ and $Y_0 \ldots Y_{31}$ with (X_0, Y_0) occurring in the bottom left corner of the matrix. The scanning process involves the orderly generation of all 1024 matrix coordinates. This is accomplished by means of a 5-bit Y Counter controlled by a clock. This counter controls a 5-bit X Counter. The X Counter is stepped up by one each time the Y Counter completes its cycle of 32 steps. In this way the matrix is scanned sequentially column by column from bottom to top.

2.2 X and Y Control

The specific coordinates are available as the outputs of two 5-bit binary decoders which have the five flipflop outputs of the counters as inputs. These two decoders are referred to as X Control and Y Control in Figure 1. One and only one of the 32 outputs of each decoder is a "1" depending on the binary number contained in the corresponding counter.

2.3 Resistance Chain

These 64 digital signals from the two decoders are changed into their corresponding analog values $-7.5 \leq X_i, Y_j \leq 8.0$ volts by means of the system shown in Figure 2.

The diamond-shaped symbol represents a diamond gate circuit (Section 2.4). It is a hybrid analog-digital circuit whose input equals its output when the gate is a "1," otherwise its output floats; gX_i and gY_j are the digital outputs of the X and Y decoders.

If V is fixed at 8 volts and if $R_1 = R_n = R_{32} = R_0$ then V_0 through V_{31} assume the values $-7.5 \leq V_n \leq 8.0$ in 0.5 volts increments. These are precisely the voltage levels corresponding to the X and Y coordinates.

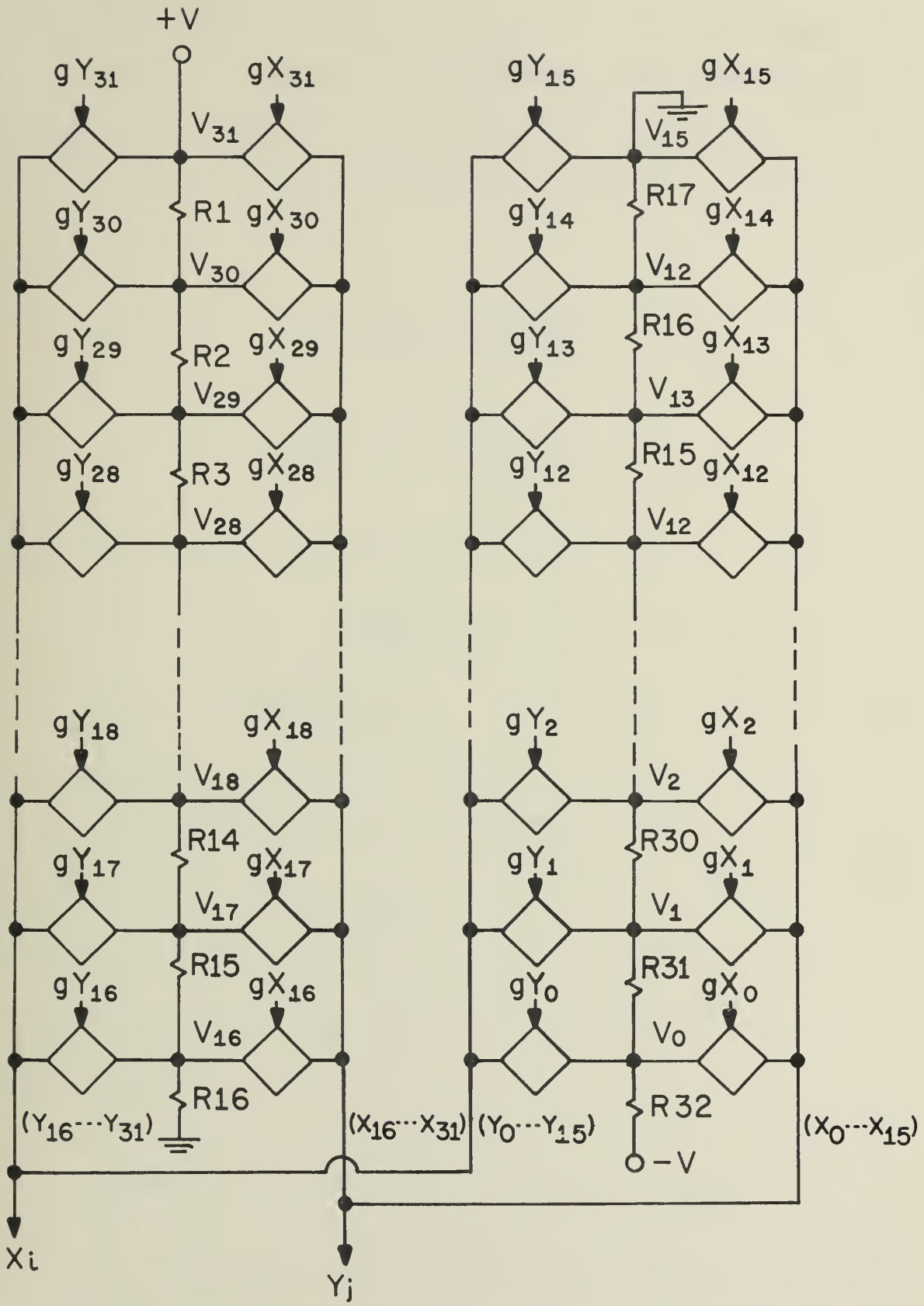


Figure 2. Resistance Chain with Diamond Gates.

Thus, if gX_i is a "1" then the X output is the analog voltage corresponding to X_i on the matrix. The Y_j output operates similarly.

The effect of a load current, I_L, can be predicted by considering the case shown in Figure 3. The dependence of V_n on n and I_L is derived as follows:

$$\frac{V - V_n}{(16-n)R_0} - \frac{V_n - 0}{nR_0} = I_L$$

$$V_n = \frac{1}{16}\left[nV - n(16-n)\, I_L\, R_0\right] .$$

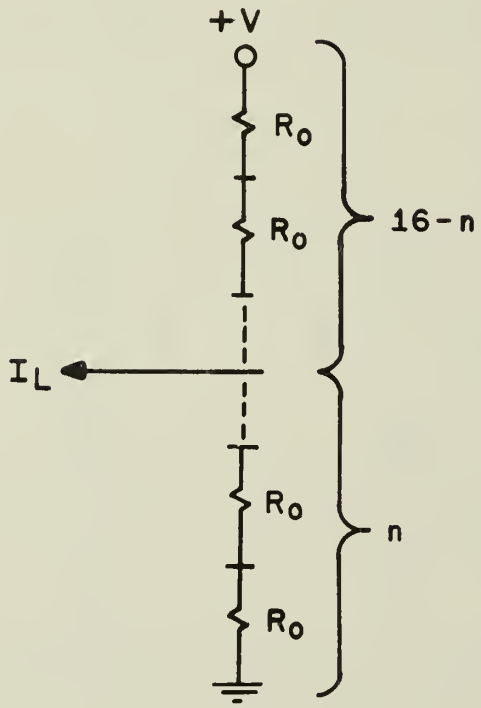


Figure 3. Resistance Chain for Tolerance Analysis.

The change in V_n due to $I_L \neq 0$ is:

$$\Delta V_n = \frac{n(16-n)\ I_L\ R_0}{16}$$

$$\Delta V_n = n\left(1 - \frac{n}{16}\right) I_L\ R_0$$

where $0 \leq n \leq 16$

$$\frac{\partial \Delta V_n}{\partial n} = I_L\ R_0\ \left(1 - \frac{2n}{16}\right)$$

$$\frac{\partial \Delta V_n}{\partial n} = I_L\ R_0\ \left(1 - \frac{n}{8}\right) .$$

ΔV_n is maximum at $n = 8$. The maximum ΔV_n is thus

$$\Delta V_{n\ max.} = 8\left(1 - \frac{8}{16}\right) I_L\ R_0$$

$$\Delta V_{n\ max.} = 4 I_L\ R_0 . \qquad (2.1)$$

The effects of variation in resistor values can be investigated by again referring to Figure 3. For worst-case analysis, the 16-n resistors are assumed to be the lowest possible and the n resistors the highest possible within the resistor tolerances. Denoting the resistor tolerance by α', $\bar{R} = R_{0\ max.}$, and $\underline{R} = R_{0\ min.}$, the equation for ΔV_n in terms of the resistor tolerance α' is:

$$V_n = \frac{n\bar{R}}{n\bar{R} + (16-n)\underline{R}}$$

$$V_n = \frac{n(1 + \alpha')\ R_0}{n(1 + \alpha')R_0 + (16-n)(1 - \alpha')\ R_0} .$$

Defining V_{n0} as V_n when $\alpha' = 0$

$$V_n - V_{n0} = \frac{nV}{16}\left[\frac{16(1+\alpha')}{n(1+\alpha') + (16-n)(1-\alpha')} - 1\right] = \Delta V'_n$$

$$\Delta V'_n = \frac{nV\alpha'}{16}\left[\frac{32-2n}{16 - 16\alpha' + 2n\alpha'}\right]$$

$$\frac{\partial \Delta V'_n}{\partial n} = (32-4n)(16 - 16\alpha' + 2n\alpha') - n(32-2n)2\alpha'$$

$$\frac{\partial \Delta V'_n}{\partial n} = 32(16)(1-\alpha') - 64n(1-\alpha') - 4n^2\alpha'.$$

Assuming the resistors will be small tolerance $\alpha' \ll 1$, $\Delta V'_n$ is then maximum at $n = 8$ and

$$\Delta V'_{n\,max} = \frac{V\alpha'}{2} \quad . \tag{2.2}$$

2.4 Diamond Gate

The diamond gate used in Figure 2 is shown in Figure 4. The inputs to the diamond are the analog voltages corresponding to the various matrix coordinates. The gate signal is the gX_i or gY_j signal from the X or Y control. These gX_i and gY_j signals are the outputs of NOR circuits and their level is either 0 volts for "1" or -5.0 volts for "0."

If the gate signal is a "1" (0 volts), $V_{in} = V_{out}$. T_1 is off since its base is well above the base of T_2. Fifteen milliamps then flows through T_2 and T_3. The diode drops are the same and $V_{in} = V_{out}$.

If the gate signal is a "0" (-5.0 volts), T_1 is on and T_2 is off since the base of T_2 is above that of T_1. Current thus flows around the diamond through R_3, T_3, and R_4. V_{out} thus floats and is restricted to the range $-10 \leq V_{out} \leq +10$ volts by the choice of base voltages of T_2 and T_3.

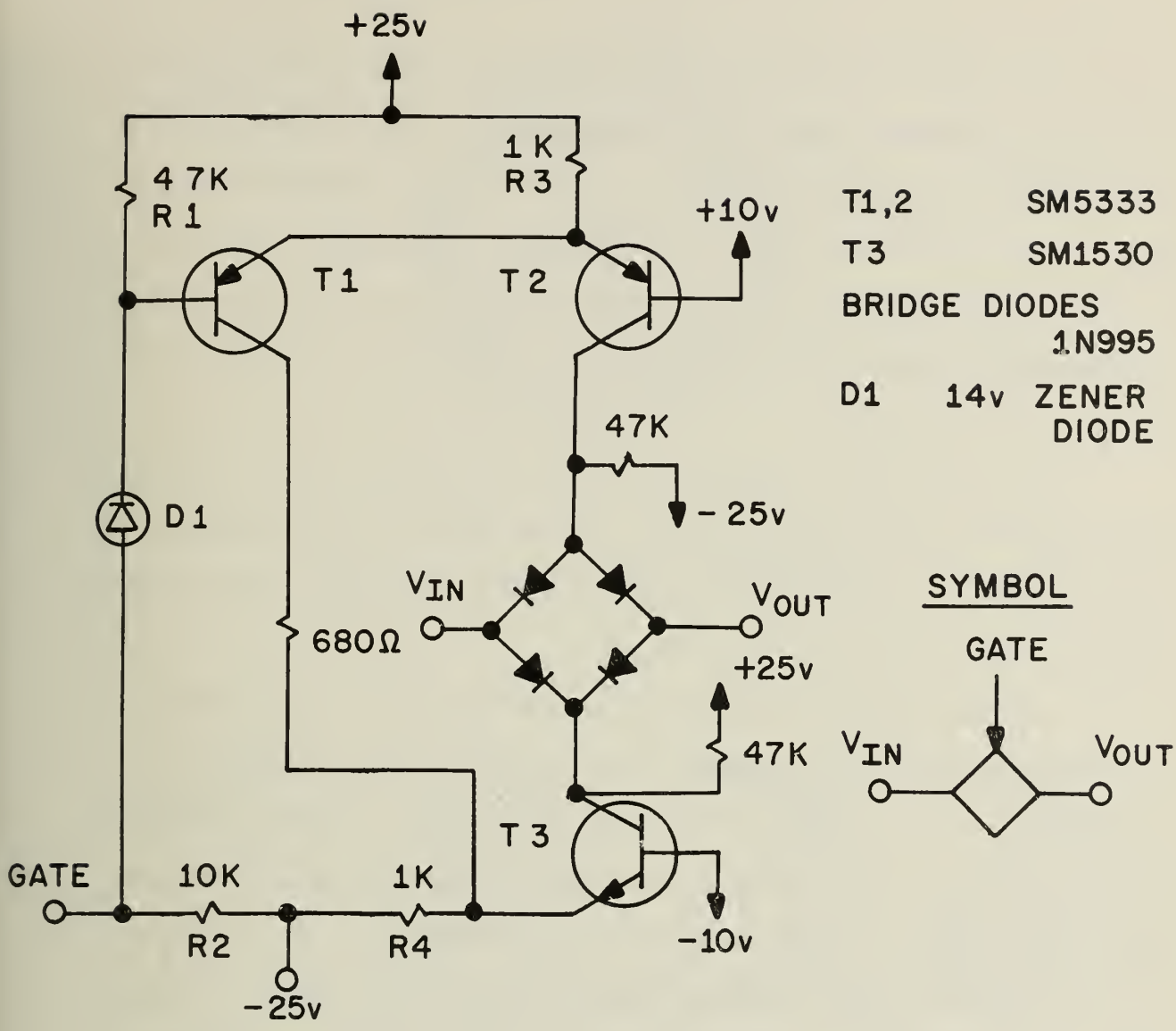


Figure 4. Diamond Gate Circuit.

3. ROTATION: SINE-COSINE POTENTIOMETER

The simplest way of accurately generating the sine and cosine of an angle is by means of a sine-cosine potentiometer. The potentiometer is wirewound with continuous rotation. It has four wipers separated by 90°. Figure 5 shows that, with inputs $\pm$ V, the outputs are $\pm$ V sin θ, $\pm$ V cos θ. The potentiometer used is accurate to within one per cent. The figure shows that the potentiometer is not wound linearly, but rather is proportional to the sine and cosine curves.

This sine-cosine potentiometer can be combined with the resistance chain to generate the rotation terms in the equations of transformation. Figure 6 shows the connections necessary. They simply involve replacing the $\pm$ 8 volts supplies by $\pm$ 8 sin θ, $\pm$ 8 cos θ.

Due to the fact that all four trigonometric values with positive and negative signs can be generated, it is not necessary to subtract two voltage levels or to attempt to invert analog signals. These two operations would be difficult to perform to the desired accuracy of less than one per cent. Such operations would also employ more circuitry.

The four outputs shown in Figure 6 are precisely the first four terms in the equations of transformation with appropriate signs already included in the generated values.

The sine-cosine potentiometer must have a fixed load if its accuracy is to be maintained. The potentiometer used has a specified fixed load of 320 Ω. Each resistor R_0 in the resistance chain is thus 20 Ω. Equation (2.2) predicts a worst-case error of 40 mv if one per cent resistors are used.

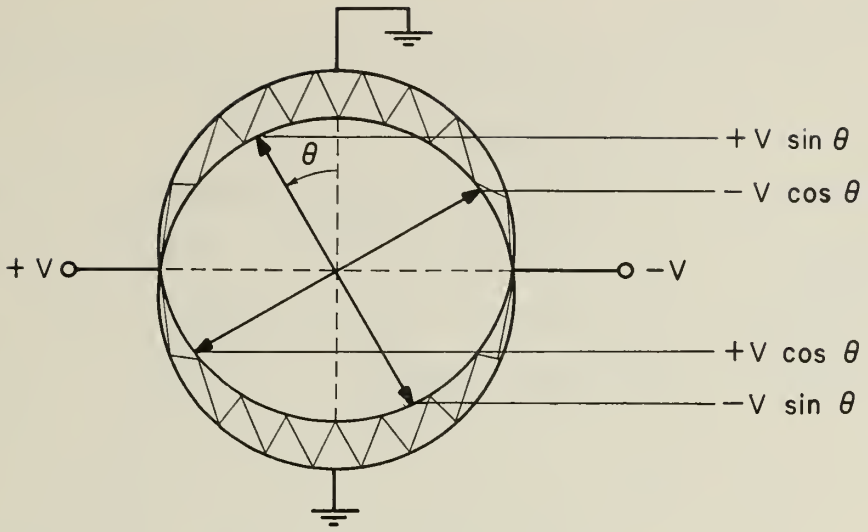


Figure 5. Sine-Cosine Potentiometer.

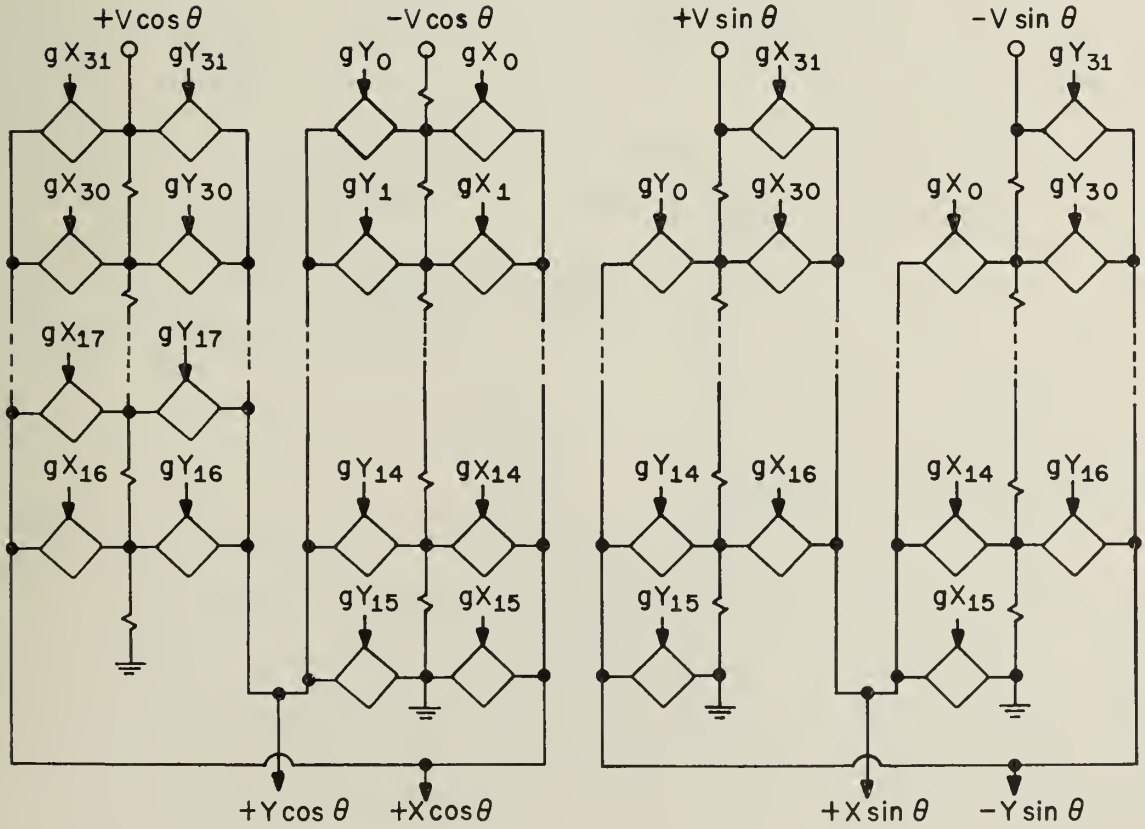


Figure 6. Resistance Chain with Sine-Cosine Potentiometer and Diamond Gates.

4.1 Current Amplifier

Before discussing the manner in which translation is achieved a current amplifier will be discussed.

At many points in this system more current was needed than the particular point in question was capable of furnishing with the desired accuracy. A simple emitter-follower would introduce too much error and thus a current amplifier was necessary, capable of furnishing or receiving 10 ma and for which $V_{in} = V_{out} \pm 50$ mv over the range $-10 \leq V_{in} \leq +10$ volts.

The circuit is shown in Figure 7 and used in Figure 8. T_1 is a constant-current source and T_7 is a constant-current sink, thus the current flowing in T_2 is constant and V_{eb2} is constant. T_5 and T_6 are a difference amplifier connected between input and output. If the output is above the input, T_6 passes more current and the bases of T_3 and T_4 are lowered thus lowering the output. Similarly, if the output is below the input, T_6 passes less current and the bases of T_3 and T_4 are raised thus raising the output. The output transistors T_3 and T_4 enable this circuit to provide or receive current. Only one output transistor is on at a time depending on whether the output is positive or negative. The output voltage is again restricted to the range $-10 \leq V_{out} \leq +10$ volts by the two collector supplies of T_3 and T_4.

4.2 Resistive Summing Network

The easiest way of adding two voltages is by means of a resistive summing network. Figure 8 shows the topology necessary to generate the equations of transformation. The four inputs to the first two resistive summing networks are the outputs of the four diamond gate chains shown in Figure 6.

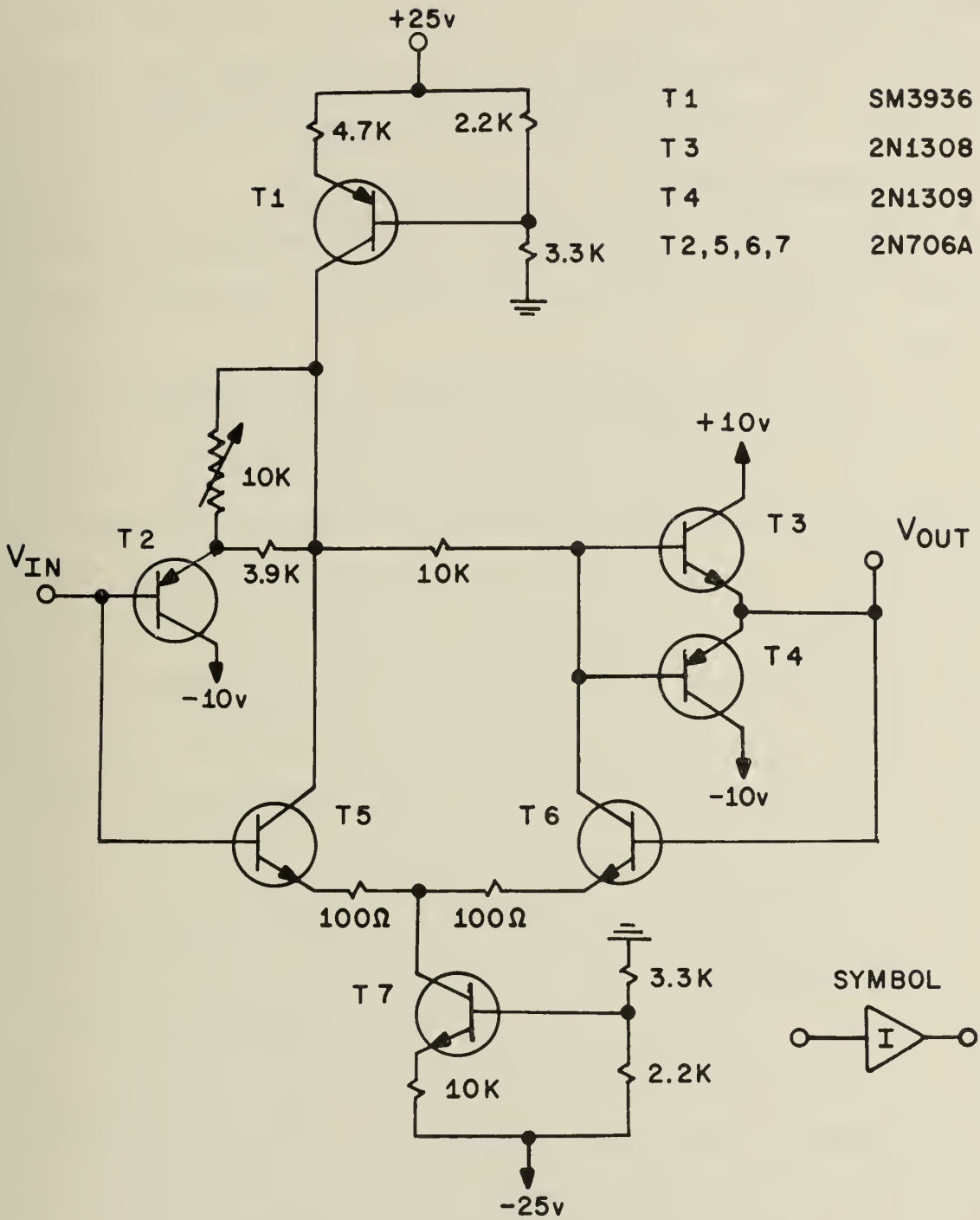


Figure 7. Current Amplifier Circuit.

Any output current from the diamond gate must be supplied at the input. The inputs to the diamond gates are points on the resistance chain. Equation (2.1) shows that for even a 1 ma load current in one diamond chain the voltages on the resistance chain are in error by as much as 80 mv. This error can easily be eliminated by inserting current amplifiers at the outputs of the four diamond gate chains as shown in Figure 8.

The error in the current amplifier is approximately 5 mv per ma of load current. The output currents will be restricted to a maximum of about 5 ma to improve accuracy.

A resistive summing network will not be accurate unless negligible current is drawn from its summing junction. The current amplifiers placed at the output of the first stage resistive summing networks insure this operating condition. It will be shown that the voltage drop across R_1 can reach a maximum of 5 volts. The current in R_1 must be limited to 10 ma due to the current amplifier and the limit chosen is 5 ma. This determines the value of R_1. The value of R_5 is variable and reaches $4R_1$ as a maximum. This prevents using widely different impedance levels for the stage 1 and stage 2 voltage dividers instead of the extra two current amplifiers.

The loss in the resistive summing network used as the second stage adder is fixed at approximately 1/2.2 and the input controlling the translation quantities a and b is varied. This was necessary since the coefficient of a and b in the equations of transformation is -1. Using a fixed source for a or b and varying the summing resistor would vary a and b as is desired but it would also vary the coefficient of the first two terms in the equations of transformation by this same variable coefficient. This would make the potentiometer settings for various values of m, n, a, and b very difficult if not impossible to determine.

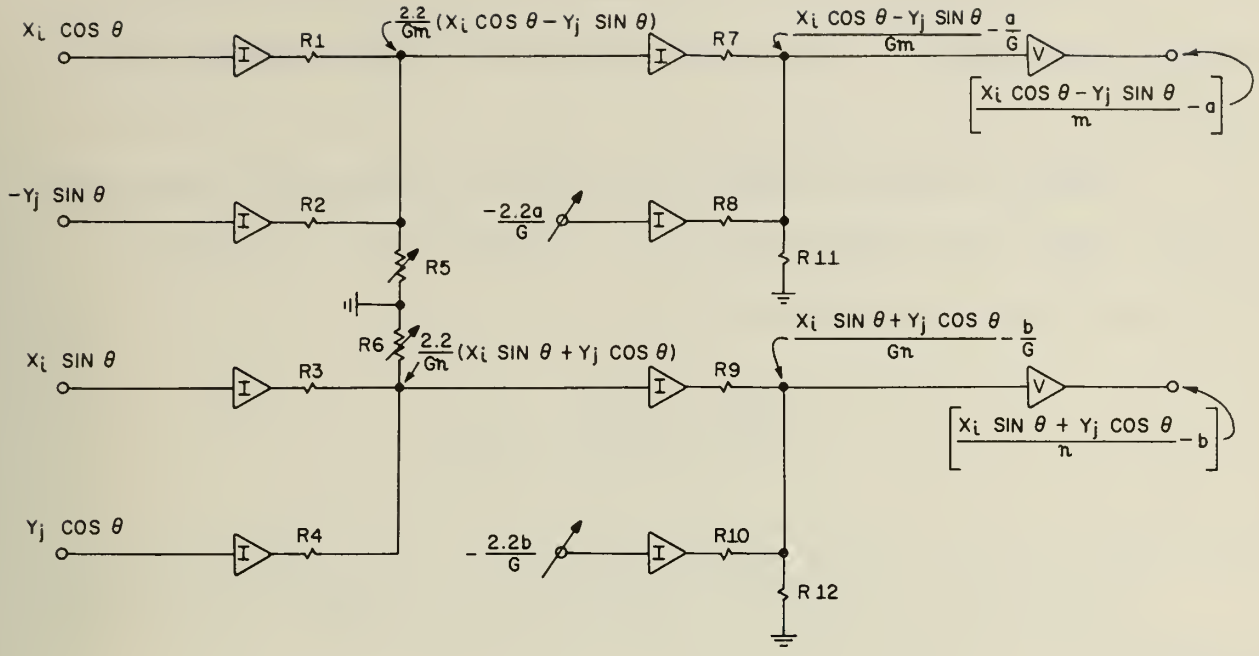


Figure 8. Translation by Voltage Dividers and Current Amplifiers.

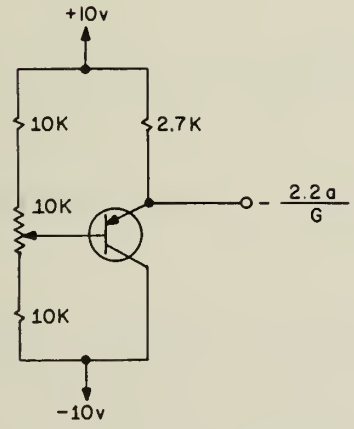


Figure 9. Translation Control.

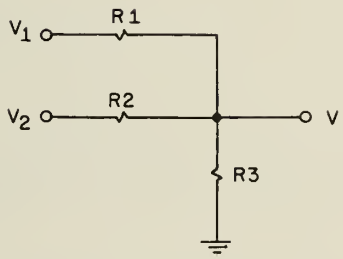


Figure 10. Voltage Divider.

Similar reasons apply to the possibility of a single resistive summing network with three inputs replacing the two-stage arrangement of Figure 8.

Figure 9 shows the simple arrangement for generating the variable voltages $-\frac{2.2}{G}a$ and $-\frac{2.2}{G}b$ where $G \approx 20$ and $-16 < a, b < +16$ volts. The voltage ranges are approximately:

$$-1.76 < -\frac{2.2}{G}a, -\frac{2.2}{G}b < +1.76 \text{ v} . \tag{4.1}$$

These supplies must be capable of furnishing 4 ma at all voltage levels.

Referring to the resistive summing network of Figure 10, the output in terms of the two inputs is

$$V = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} . \tag{4.2}$$

Choosing $R_1 = R_2$

$$V = (V_1 + V_2)\frac{R_3}{R_1 + 2R_3} . \tag{4.3}$$

The term $R_3/(R_1 + 2R_3)$ is defined as the resistive summing network coefficient, K.

Referring to Figure 8, the coefficient for the first stage summing network is $K_1 = 2.2/(Gm)$ where $G \approx 20$ and $1/4 \leq m \leq 4$. Thus the range of K_1 becomes

$$.0275 \leq K_1 \leq .44 \tag{4.4}$$

The coefficient, K_1, is restricted to the range $0 \leq K_1 \leq 1/2$. Equation (4.4) shows that K_1 does satisfy this inequality. The value of K_2, the coefficient for the second stage resistive summing network, was chosen as 1/2.2 to insure that K_1 for the first stage resistive summing network is within the allowed range since $1/K_2$ appears in K_1. For the model of Figure 10 the inequalities become

$$.0275 \leq \frac{R_3}{R_1 + 2R_3} \leq .44 \tag{4.5}$$

or

$$.0291\ R_1 \leq R_3 \leq 3.67\ R_1 \ . \tag{4.6}$$

The maximum value of V_{R_1}, the voltage across R_1, will be:

$$\frac{2.2}{20(.25)} \left[X_i \cos\theta - Y_j \sin\theta\right]_{max.}$$

It can easily be shown that

$$\left[\binom{X}{Y} \cos\theta \mp \binom{Y}{X} \sin\theta\right]_{max.} = \pm \left[\sqrt{X^2 + Y^2}\right]_{max.}$$

$$= \pm\ 8\sqrt{2} \approx \pm\ 11.3\ \text{v} \ . \tag{4.7}$$

Thus,

$$V_{R_1\ max.} \approx \frac{2.2}{20} \ \frac{11.3}{.25} \approx \pm\ 4.95\ \text{v} \ . \tag{4.8}$$

The voltage across R_7 in Figure 8 is

$$V_{R_7} = X_i (1 - K_1) \cos \theta + Y_j K_1 \sin \theta$$

$$V_{R_7 \text{ max.}} = 4\sqrt{2} \approx 6 \text{ v} . \qquad (4.9)$$

If $R_1 = R_2 = R_3 = R_4 = 1K$ the load current of the four current amplifiers is restricted to

$$0 \leq I_L \leq 6 \text{ ma} . \qquad (4.10)$$

The first stage summing resistors must vary in the range

$$27.5 \ \Omega \leq R_5, R_6 \leq 4.6 \text{ K } \Omega . \qquad (4.11)$$

By a similar analysis the second stage voltage divider resistor values are

$$R_7 = R_8 = R_9 = R_{10} = 500 \ \Omega$$

$$R_{11} = R_{12} = 2.5 \text{ K } \Omega$$

The base currents of the current amplifier will be constant since the current in the input transistor is constant and under proper operation the current in the feedback difference amplifier will be constant. This means that whatever base current flows, it is constant. Its amplitude has been measured as only 5 μa but with m = 4 this flows into a 4.4 K Ω summing resistor and thus produces a 22 mv error. This can be corrected by adjusting the summing resistors.

Since resistive summing networks are used and the input resistors are equal, the coefficient K is always less than 1/n where n is the number of inputs. Such a network cannot give gain and since the required gain 1/m lies in the range

$$\frac{1}{4} \leq \frac{1}{m} \leq 4 \qquad (4.12)$$

a voltage amplifier is necessary. Its gain has been assumed to be about 20. It is symbolized in Figure 8 by

.

The resistors in the first stage voltage divider could be fixed and then the problem would become one of designing a highly accurate and fast voltage amplifier capable of an output range $-10 \leq V_{out} \leq +10$ volts with the additional stipulation that the gain be variable. It is far more direct to vary the summing resistor in the resistor adder and keep the gain of the voltage amplifier constant.

The remainder of this thesis will be devoted to an extensive analysis of such a voltage amplifier.

5. MAGNIFICATION: VOLTAGE AMPLIFIER

5.1 Specifications

The voltage amplifier necessary must conform to the following specifications:

(1) A high input impedance,

(2) An output capable of supplying 10 ma,

(3) An output range of $-10 \leq V_{out} \leq +10$ volts,

(4) A frequency range of d-c to 1 mc,

(5) A constant gain of about 20 with an error of less than one per cent over the entire voltage range,

(6) A drift of less than 30 mv over the entire voltage range,

(7) An output offset voltage of less than 10 mv when the input is switched from any level to ground, and

(8) The capability of interchange of components with no loss of accuracy.

It is also desirable that this circuit be uncomplicated. No special components will be used such as matched transistor pairs, thermistors, temperature sensing diodes, or hot or cold ovens. In other words the circuit should be simple, and the topolcgy and not the components should be the basis for the accuracy.

5.2 Methods of Amplification

Many d-c amplifiers employ operational amplifiers with parallel feedback and the gain is then the ratio of feedback resistance to input resistance if the gain of the amplifier is of the order of 10^5.

Amplifiers capable of responding to direct current or voltage present many problems. Resistive coupling of several amplifier stages produces an amplifier which responds to direct current or voltage. However, such amplifiers cannot distinguish between signals generated externally or signals generated internally. A change in V_{eb} or I_{cbO} is amplified as readily as an input signal. An amplifier which responds only to a-c signals does not have this cumulative drift-error. For this reason, normally when very accurate d-c amplifiers are desired, the input d-c signal is changed into an a-c signal by means of a transistor chopper. The a-c signal is then amplified and then rectified for a d-c output.

Another newly developed method of amplification of d-c levels fairly accurately and over wide frequency ranges is that of integrated circuitry. With present techniques transistor parameters can be made equal within 0.01 per cent. Transistors can be made on the same block and all elements are thus at the same temperature and thermal problems are greatly reduced. In this manner very drift-free circuits can be produced.

Such methods are not readily available, and methods employing transistor choppers and rectifiers, many of which employ matched transistor pairs to cancel leakage currents and parameter variations, require very much circuitry.

5.3 Sources of Drift

The method of introduction to the final amplifier design will be to state the well known transistor phenomena which produce drift and loss of accuracy. The merits of various methods of compensating these errors will be discussed. In this way the best theoretical input stage and a novel output stage will be developed. From these observations the final circuit topology will be produced.

The major reasons for drift in a transistor are variations in the d-c properties of the collector-base and emitter-base diodes and the d-c transfer ratio. The T-equivalent circuit for a transistor is shown in Figure 11.

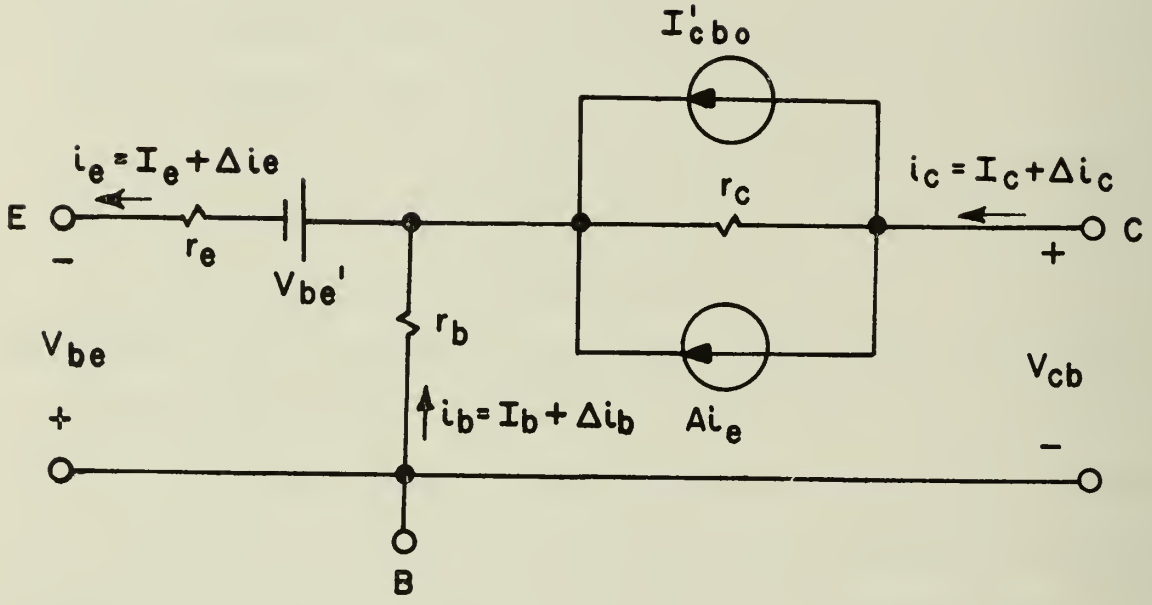


Figure 11. T-Equivalent Transistor Circuit.

The parameters r_e, r_b, r_c and α are the conventional small signal parameters at the operating point. The battery V'_{be}, generator I'_{c0}, and d-c transfer ratio $\bar{\alpha}$ provide necessary current and voltage for the operating point. The currents denoted by capital letters are quiescent values and the deviations from these values are denoted by Δi.

From Figure 11:

$$V_{be} = V'_{be} + I_b r_b + I_e r_e \qquad (5.1)$$

$$I_{cbO} = I'_{cbO} + V_{cb}/r_c \tag{5.2}$$

$$Ai_e = \bar{\alpha} I_e + \alpha \Delta i_e \quad . \tag{5.3}$$

Thus, as the emitter current or the collector current vary, V_{be}, I_{cbO}, and A vary. This fact is well known. Various biasing methods involving current and voltage feedback and other techniques have been used to reduce these variations.

One other factor of great importance is that of power dissipation. It is a known fact that as the power dissipation at the collector junction increases the junction temperature, T_j, will increase causing a ΔV_{eb} and a ΔI_{cO}. If the collector junction does not remain at the ambient temperature, T_a, the operating point will shift. This effect can be minimized by choosing transistors with reasonable I_{cO} and thermal conductivity and circuits with low power, low voltage, and low stability factor, S.

Negative feedback has been found to be very useful in amplifier design. It possesses three well known properties:

(1) It increases stability,

(2) It reduces frequency and phase distortion, and

(3) It reduces nonlinear distortion.

Local current and voltage feedback are frequently used in d-c amplifiers. Before proceeding further three stability parameters will be defined.

(1) Input voltage drift is the change in input voltage required to maintain constant output conditions when the parameters of the circuit vary.

(2) Input current drift is the change in input current required to maintain constant output conditions when the parameters of the circuit vary.

(3) Stability, S, is the ratio of the change in collector current to the change in I_{c0}.

5.4 Input Stage

Figure 12 shows the equivalent circuit for a typical NPN difference d-c amplifier stage. The equivalent input voltage drift is

$$\Delta V_1 - \Delta V_2 = -(\Delta V_{be1} - \Delta V_{be2}) - \frac{R_b + r_b + R_e + r_e}{\alpha}(\Delta I_{cb01} - \Delta I_{cb02}) - \frac{R_b + r_b + R_e + r_e}{\alpha}(\Delta \bar{\alpha}_1 I_{e1} - \Delta \bar{\alpha}_2 I_{e2}) . \tag{5.4}$$

This expression is similar to that for a single-ended stage, however, now any error due to parameter variations is reduced appreciably since in the differential arrangement the corresponding parameters of the two transistors are subtractive. By choosing suitable circuit values, this drift can be made very small.

Such drift reduction by compensation does not materially affect the gain and thus produces a noticeable improvement in the minimum detectable input signal. This should be contrasted to other methods of stabilization involving local degeneration which reduces the gain and decreases the minimum detectable signal.

The stability, S, of each side of the difference amplifier of Figure 13 can be calculated to be

$$S = \frac{\partial I_c}{\partial I_{c0}} = \frac{2R_e + R_b}{2R_e + R_b(1 - \alpha)} . \tag{5.5}$$

However, if the parameters of the two transistors are not balanced, the emitter resistance of each side will be the parallel combination

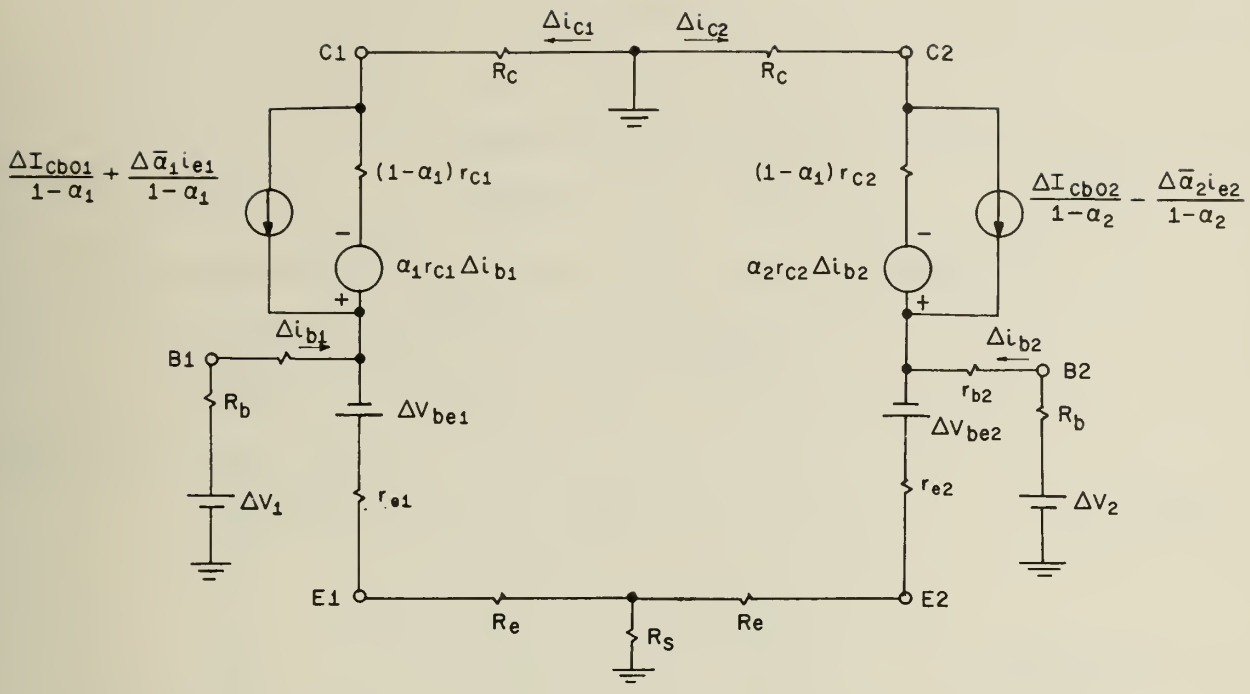


Figure 12. Drift Equivalent Circuit for NPN Difference Amplifier.

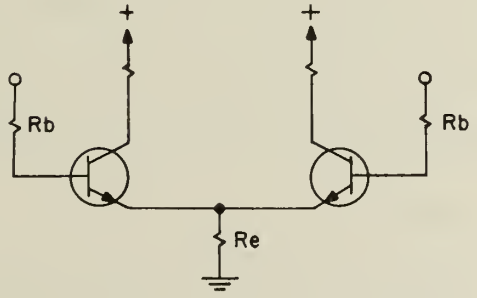


Figure 13. NPN Difference Amplifier for Stability Analysis.

of R_e and $R_b/(\beta + 1)$. The effective emitter resistance is thus $R_b/(\beta + 1)$. The worst-case stability factor is then $\beta/2$.

It can be concluded that the best input stage would be a difference amplifier with negative feedback applied appropriately in the input stage. The input drift of a differential stage has been found to be much better than that of an equivalent single-ended stage. This improvement can be partly attributed to the inherent consistency of $\Delta V_{eb}/\Delta T$ coefficients which, for unmatched transistors of a given type, differ by less than ten per cent. Other similar benefits occur. If the currents in this input stage are restricted to low values the drift will be further reduced.

5.5 Second Stage

A simple second stage as shown in Figure 14 produced interesting benefits. Figure 14 is shown with values of drift in stages 1 and 2. For clarity at present, stage 1 is shown as a single-ended amplifier. Figure 14 shows the effect of second stage drift referred to the first stage. For the single-ended first stage amplifier shown, the current and voltage drifts of stage 2 tend to cancel those of stage 1. For a normal difference amplifier the stage 2 drift may add or oppose the first stage drift.

The minimization of the drift in stage 1 is very important since any drift present will be multiplied by the gain of stage 2.

5.6 Output Stage

Past attempts at such an amplifier with an open-loop gain greater than 100 reduced by feedback to a closed-loop gain of about 20 were accurate to about three per cent and commonly possessed drifts of about 150 mv. The obvious reason for this drift and nonlinearity was the fact that the output of this amplifier had a range of 20 volts and had to be capable of handling

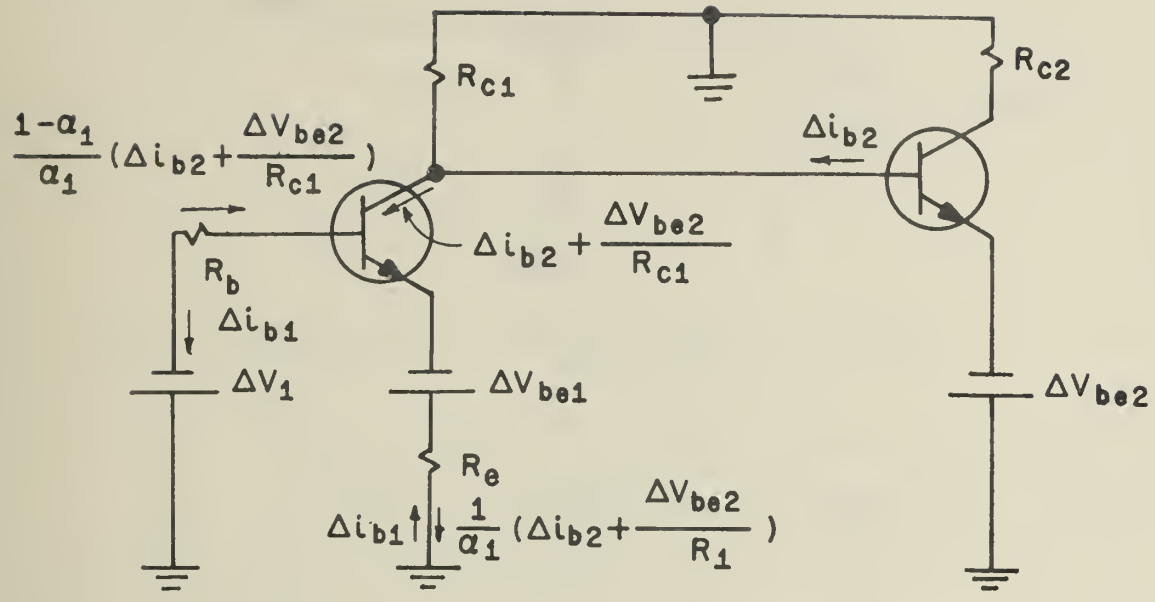


Figure 14. Drift Currents and Voltages in Two-Stage Amplifier.

both positive and negative voltages. When the output was changed from its maximum positive value to its maximum negative value, every transistor junction in the circuit either went from its highest temperature to its lowest or vice versa. Under such conditions all transistor parameters changed by their greatest amount and many of these changes were magnified in one or the other or both of the amplifier stages. These problems are typical of most d-c amplifiers. The solution chosen was the novel output stage shown in Figure 15.

The voltage V_1 is the output of a two-stage amplifier similar to Figure 14. The voltage V_2 is the output of a similar two-stage amplifier but with the polarity of all transistors reversed. The voltages V_1 and V_2 are chosen such that at V_{in} = 0 volts; the voltage drop across the

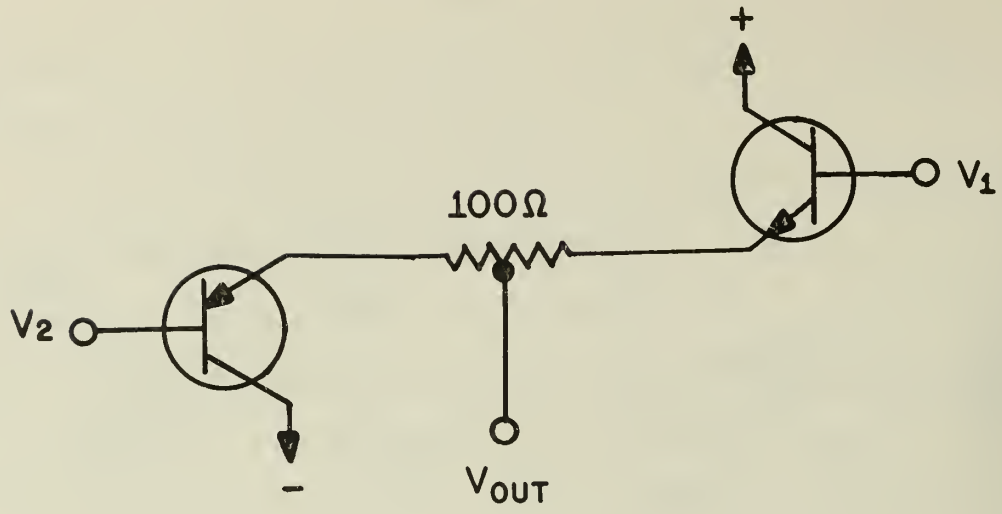
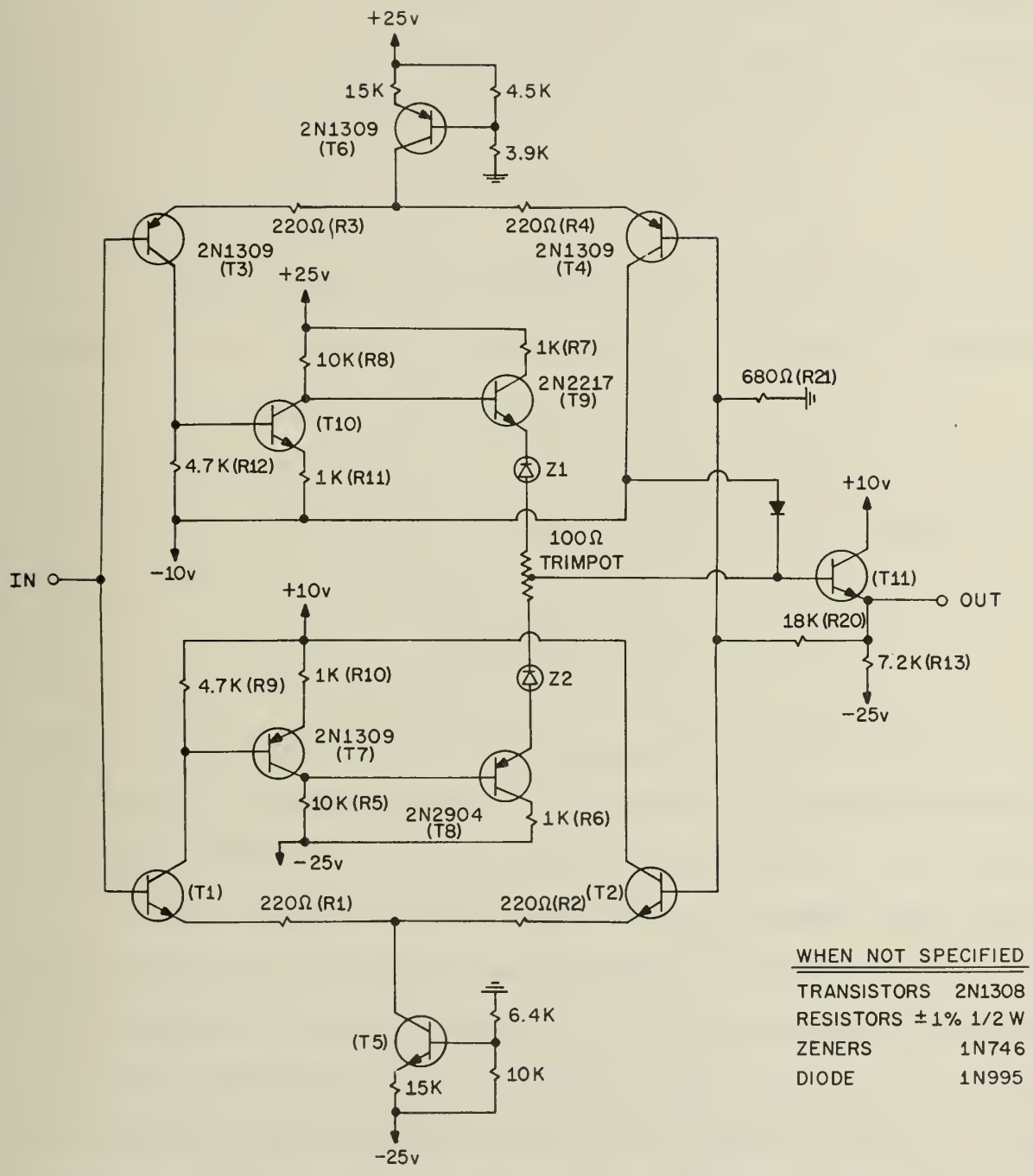


Figure 15. Constant-Current Output Stage.

potentiometer is 1.0 volts. Since V_1 and V_2 are the outputs of two similar two-stage amplifiers, the inputs of both amplifiers may be connected with the result that for a given increment in input voltage V_1 and V_2 increase by approximately equal increments depending on the equality of their respective gains. This maintains a constant voltage across the potentiometer and thus the current through both transistors is constant and the V_{eb} drops of both transistors are constant. The output wiper can be adjusted at $V_{in} = 0$ to give $V_{out} = 0$. Thereafter $V_{out} = K (V_1 + V_2)$ where K is a constant and depends on the position on the potentiometer where the wiper is placed. This circuit is called a constant-current output stage.

5.7 Amplifier Topology

The amplifier is shown in Figure 16 with resistor values and the transistor types used in this application. As noted previously, it is composed of two similar two-stage amplifiers whose output voltages are offset by a constant amount feeding the modified output stage of Figure 15 which goes through an emitter-follower whose output is fed back to the two non-input bases of the two difference amplifiers with negative feedback. It has an open-loop gain of 107 and a closed-loop gain of about 21.



WHEN NOT SPECIFIED	
TRANSISTORS	2N1308
RESISTORS	±1% 1/2 W
ZENERS	1N746
DIODE	1N995

Figure 16. Ultralinear Voltage Amplifier.

Equation (5.4) demonstrated the low input-voltage drift possible with this input stage. Due to the negative feedback, the insertion of resistors directly in the emitters of the difference amplifier transistors to drastically reduce any difference in r_e and to improve linearity, the choice of transistors with $\beta > 50$, and the use of constant-current drive in place of a resistor returned to a supply voltage, equation (5.5) can be used to calculate the stability. The value of R_e in equation (5.5) now becomes

$$R_e \approx r_c + (\beta + 1) R'_e \tag{5.6}$$

due to the constant-current drive, where R'_e is the external emitter resistance of the constant-current generator. Using the values of Figure 16

$$R_e \approx 2 \text{ M}\Omega \tag{5.7}$$

and the stability, S, of the input stage is found to be

$$S \approx \frac{4 \times 10^6 + 10^3}{4 \times 10^6 + 20} \tag{5.8}$$

The second stage of the amplifier consists of T_{10}, R_8, R_{11} for one amplifier and T_7, R_{10}, R_5 for the other. The feedback ratio is chosen to be greater than the final gain of the amplifier as will be shown later. This fact means that the input transistor's base voltage varies by a larger increment than does the base voltage controlled by the feedback. This enables the input stage which is actually a difference amplifier to be treated as a single-ended amplifier as far as the investigation and effect of voltage and current drift are concerned, yet as a difference amplifier as far as compensation is concerned. The two stages thus have the same properties as the two-stage amplifier of Figure 14, namely that any drift voltage or current from the second stage tends to cancel the drift

voltage and current of the first stage thus creating a quite stable input stage. The first stage gain of each amplifier should be very nearly the same and quite linear.

The feedback is such as to properly compensate for any errors due to parameter variations. If the output voltage is too high, the bases of T_4 and T_2 will be too high, decreasing the current in R_4 and increasing the current in R_2. This causes the current in T_3 to increase and in T_1 to decrease. The bases of T_{10} and T_7 rise, causing the bases of T_8 and T_9 to fall which reduces the output. This is the desired effect for the chosen case of too high an output. The feedback works similarly to increase an output which is too low.

The stability of the second stage gain will be discussed in conjunction with the output stage. The fairly linear gains of both two-stage amplifiers will keep the initial offset voltage between the bases of T_8 and T_9 rather constant. This constant difference maintains the emitter currents of T_8 and T_9 at constant values and thus V_{eb8} and V_{eb9} remain nearly constant. The resistors R_6 and R_7 merely serve to fix the two collectors at convenient points where $V_{cb\ min.}$ cannot be reached and the value of V_{cb} can be kept as low as possible without using two additional power supplies and connecting the collectors directly to them.

This topology produces a circuit which is thermally quite stable despite the large voltage ranges. The magnitude of the current sources are chosen such that the portion of the V_{eb} versus I_c curve which is used can quite easily be linearized. This was necessary since over the voltage range necessary it was impossible to completely cancel V_{eb} between transistors although the differential input stage employed does this to a great extent.

A more rigorous treatment of the thermal stability of the circuit appears in Sections 5.12, 5.13, and 5.14. The effect of V_{eb} variations on linearity is treated similarly in Sections 5.10 and 5.11.

The gain of the first stage is about 10, reduced by feedback to about 2, the second stage gain is 10.

5.8 Emitter-Follower Output

The reason for the output NPN emitter-follower T_{11} can be seen from a consideration of the driving capabilities of the output of Figure 15. The output circuit is redrawn in Figure 17 with the feedback resistor R_{20} of Figure 16 as shown.

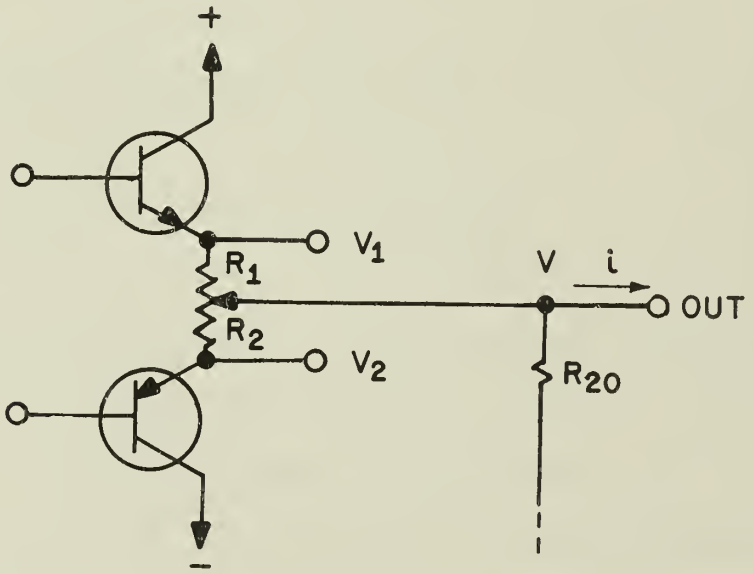


Figure 17. Loaded Output Stage.

The effect of a load current on the output can be determined from the following equation:

$$\frac{V_1 - V}{R_1} - i = \frac{V - V_2}{R_2} .$$

Let the potentiometer resistance be R_0 and define K such that

$$R_1 + R_2 = R_0$$

$$R_1 = K R_0$$

$$R_2 = (1 - K) R_0$$

$$V = V_1 - V_1K + V_2K - KR_0(1 - K)i \ .$$

The quantity $V_1 - V_1K + V_2K$ is the theoretical value of V_{out}.

$$V_{out} - V = \Delta V_{out} = KR_0(1 - K)i = \text{loading error} \ . \qquad (5.9)$$

The smaller R_0 or K is made, the smaller the loading error becomes since the output impedance thus decreases.

With the following values:

$$i = 10 \text{ ma}$$

$$R_0 = 50 \ \Omega$$

$$K = 1/10 \ ,$$

equation (5.9) becomes

$$\text{loading error} = 45 \text{ mv} \ .$$

Equation (5.9) has not considered the effect of an output change on the circuit feedback. Referring to Figure 16, a load current causes the base of T_8 to increase, causing the base of T_7 to decrease, the collector current of T_1 to increase. The effect through T_1 and T_2 is multiplied by the feedback ratio and added to the above loading error. Experiments have shown that the loading error is roughly twice that predicted by equation (5.9).

The difficulty involved in setting V_1 and V_2 of Figure 17 such that K = 1/10 and the fact that the error due to loading alone will be about 90 mv leads to the conclusion that this output must be fed through an emitter-follower with feedback as in Figure 16. The potentiometer is then centered such that at V_{in} = 0 volts the emitter-follower output, V_{out}, is also 0 volts.

The fact that the output is not taken directly from the potentiometer does not affect the usefulness of and necessity for this circuit. The drift of one of the two-stage amplifiers with a similar emitter-follower output and the same feedback but without the constant-current output stage, was found to be about 150 mv. It is the constant-current output stage which reduces the drift and permits compensation.

A d-c analysis of a single two-stage amplifier employed in the voltage amplifier of Figure 16 will be presented followed by a rigorous analysis of the effect of V_{eb} and its variations on the gain and on the linearity. This amplifier is shown in Figure 18.

5.9 D-C Analysis

In this analysis it is assumed for simplicity that all transistors have V_{eb} = 0 and α = 1. Such a first order analysis investigates the basic design equations of the amplifier and the various inequalities to be satisfied.

The input voltage is U, the output voltage is V, and the current in T_n is denoted by i_n.

The current i_1 is constant

$$i_1 = \frac{R_2 Z}{R_1(R_2 + R_3)} \tag{5.10}$$

The voltage at the base of T_2 is fV where f is the feedback ratio or the fraction of output voltage fed back to T_2.

$$f = \frac{R_9}{R_9 + R_{10}} \quad . \tag{5.11}$$

The current i_3 is thus

$$U - R_5 i_3 = fV - R_4(i_1 - i_3) \tag{5.12}$$

$$i_3 = \frac{U - fV + R_4 i_1}{R_4 + R_5} \quad . \tag{5.13}$$

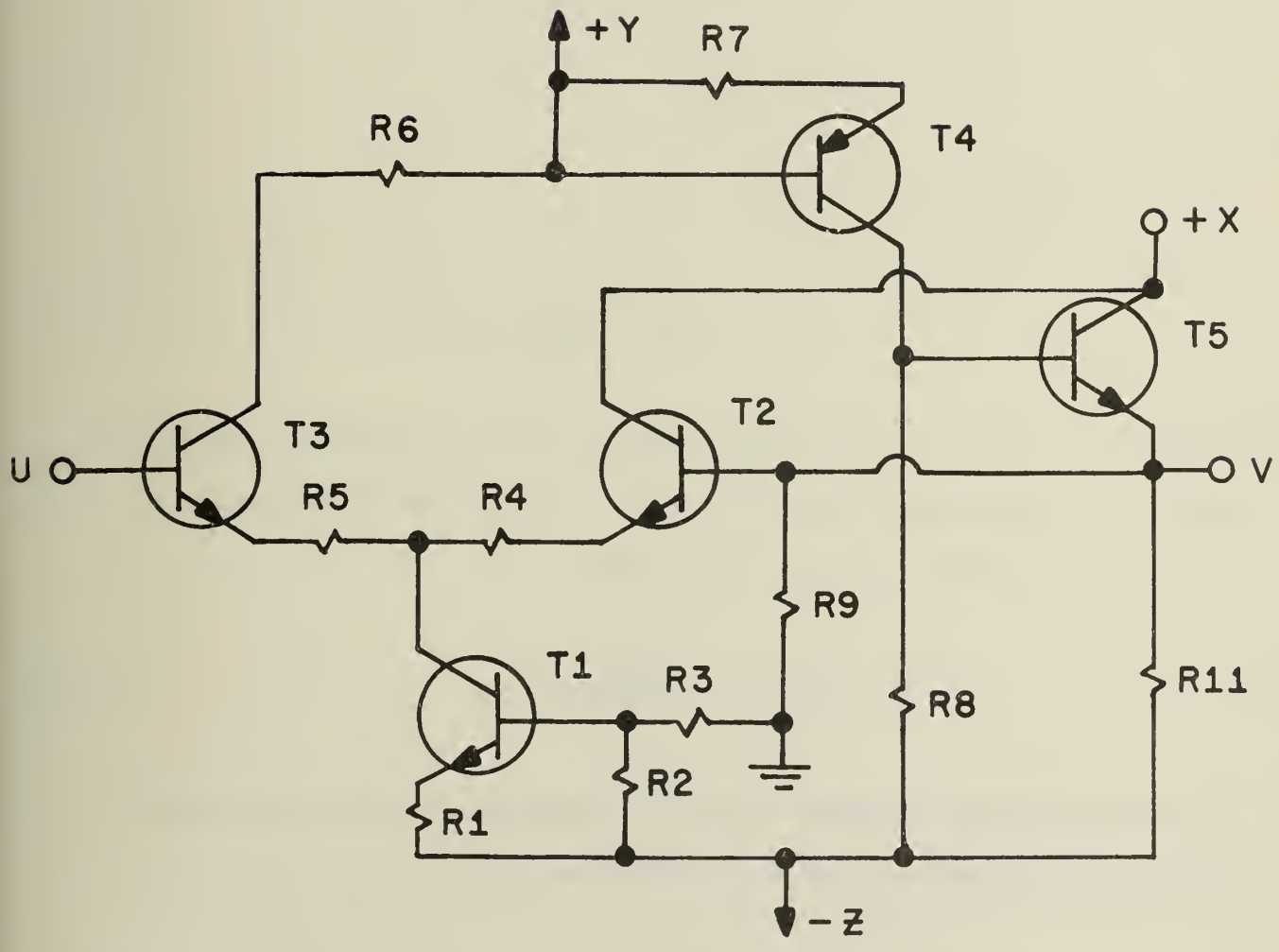


Figure 18. Two-Stage V-Amplifier for D-C Analysis.

i_4 is related to i_3 by

$$i_4 = \frac{R_6}{R_7} i_3 \quad . \tag{5.14}$$

The current i_4 determines the output voltage V.

$$V = -Z + R_8 i_4$$

$$V = -Z + \frac{R_6 R_8}{R_7} i_3 \quad \text{from (5.14)}$$

$$V = -Z + \frac{R_6 R_8}{R_7} \left(\frac{U - fV + R_4 i_1}{R_4 + R_5}\right) \quad \text{from (5.13)}$$

$$V = -Z + G_0(U - fV + R_4 i_1) \tag{5.15}$$

where G_0 is defined as the open-loop gain.

$$G_0 = \frac{R_6 R_8}{R_7(R_4 + R_5)} \quad . \tag{5.16}$$

Equation (5.16) can be verified by noting that the gain through a difference amplifier with the second base grounded is the ratio of the collector resistor to the sum of the two emitter resistors

$$G_1 = - \frac{R_6}{R_4 + R_5} \tag{5.17}$$

The second stage gain through the simple transistor stage is approximately the ratio of collector resistor to emitter resistor.

$$G_2 = - \frac{R_8}{R_7} \tag{5.18}$$

The total gain is

$$G_0 = G_1 \cdot G_2 = \frac{R_6 R_8}{R_7(R_4 + R_5)} \tag{5.19}$$

which agrees with equation (5.16). Solving equation (5.15) for V, the result is:

$$V = \frac{-Z + G_0(U + R_4 i_1)}{1 + f G_0}$$

$$V = G(U + R_4 i_1 - \frac{Z}{G_0}) \tag{5.20}$$

where G is the closed-loop gain defined as

$$G = \frac{G_0}{1 + f G_0} \quad . \tag{5.21}$$

Zero offset is defined as V = 0 when U = 0. From equations (5.10) and (5.20) the condition for zero offset becomes

$$i_1 = \frac{Z}{G_0 R_4} = \frac{Z R_2}{R_1(R_2 + R_3)} \tag{5.22}$$

or

$$\frac{(R_4 + R_5) R_7}{R_6 R_8} = \frac{R_2 R_4}{R_1(R_2 + R_3)} \quad . \tag{5.23}$$

It is very interesting to note that this offset condition is independent of all supply voltages. If $R_4 = R_5$, the offset condition is

$$\frac{R_3}{R_2} = \frac{R_6 R_8}{2R_1 R_7} - 1 \quad . \tag{5.24}$$

In the final amplifier, this offset is not zero and is adjusted by means of the constant-current source I_1.

The condition that the voltage range at the base of the input transistor T_3 be larger than the voltage range at the base of the second transistor T_2 is easily verified. The voltage range on T_3 is $-\frac{V}{G} \leq U \leq +\frac{V}{G}$ and the voltage range on T_2 is $-fV \leq U \leq +fV$. Thus the first inequality to be satisfied is

$$V\left[\frac{1}{G} - f\right] > 0 \tag{5.25}$$

or

$$\frac{1}{G} - f > 0 \ . \tag{5.26}$$

From equation (5.21)

$$\frac{1}{G} = \frac{1 + f G_0}{G_0}$$

$$\frac{1}{G} = \frac{1}{G_0} + f$$

$$\frac{1}{G} - f = \frac{1}{G_0} \ . \tag{5.27}$$

G_0 is the open-loop gain of the amplifier which is greater than zero thus

$$\frac{1}{G} - f = \frac{1}{G_0} > 0 \tag{5.28}$$

and the analysis of Section 5.5 is valid.

For T_4 and T_5 to conduct, the emitter supply of T_4 must be greater than or equal to the collector supply of T_5. This is true since the supplies chosen show

$$V = X \quad . \tag{5.29}$$

The output range over which the gain is linear is

$$-X \leq V \leq +X \tag{5.30}$$

The corresponding input range is

$$-\frac{X}{G} \leq U \leq +\frac{X}{G} \tag{5.31}$$

Now all transistors must conduct over the ranges defined by equations (5.30) and (5.31) to insure linearity of gain. When U is at its minimum value, -X/G, the linear operation condition is $i_3 > 0$, which, from equation (5.13) becomes

$$U_{min} - fV_{min} + R_4 i_1 > 0 \tag{5.32}$$

or

$$-\frac{X}{G} + fX + R_4 i_1 > 0 \quad . \tag{5.33}$$

Equation (5.28) can now be written as

$$X\left(\frac{1}{G} - f\right) = X\left(-\frac{1}{G_0}\right) \quad .$$

Equation (5.33) thus becomes

$$R_4 i_1 > X\left(\frac{1}{G} - f\right) \tag{5.34}$$

or

$$R_4 i_1 > X\left(\frac{1}{G_0}\right) \tag{5.35}$$

The zero offset condition requires

$$R_4 \, i_1 = \frac{Z}{G_0} \tag{5.36}$$

by which equation (5.35) is

$$\frac{Z}{G_0} > \frac{X}{G_0} \tag{5.37}$$

which satisfies the condition that $i_3 > 0$. The condition for this is the same as that of equation (5.29) if the collectors of T_2 and T_5 are returned to the same supply voltage.

If U is at its maximum value the linear operation condition is $i_3 < i_1$. T_4 conducts, thus $R_6 \, i_3 < Y - X$

$$R_6 \, i_3 < \text{minimum of } [R_6 \, i_1, \; Y - X] \tag{5.38}$$

From equation (5.13)

$$R_6 \, i_3 = \frac{R_6}{R_4 + R_5} \left(\frac{X}{G} - fX + \frac{Z}{G_0}\right) \tag{5.39}$$

and from equation (5.36)

$$i_1 = \frac{Z}{G_0 \, R_4} \, . \tag{5.40}$$

Equation (5.38) now has the form:

$$\begin{aligned} R_6 \, i_3 &= \frac{R_6}{R_4 + R_5} \left(\frac{X}{G} - fX + \frac{Z}{G_0}\right) \\ &< \text{minimum of } [Y - X, \; \frac{R_6 \, Z}{G_0 \, R_4}] \end{aligned} \tag{5.41}$$

or

$$\frac{R_6}{R_4 + R_5}\left(\frac{X}{G_0} + \frac{Z}{G_0}\right) < \text{minimum of } \left[Y - X, \frac{R_6}{G_0}\frac{Z}{R_4}\right] . \tag{5.42}$$

Equation (5.42) requires

$$R_6(X + Z) < R_6\, Z\left(1 + \frac{R_5}{R_4}\right) \tag{5.43}$$

or

$$\frac{R_5}{R_4} < \frac{Z}{X} . \tag{5.44}$$

Equation (5.42) also requires

$$\frac{(X + Z)R_6}{R_4 + R_5} < (Y - X)G_0 \tag{5.45}$$

or

$$(X + Z)\frac{R_7}{R_8} < Y - X . \tag{5.46}$$

As used in the final amplifier design the point V of Figure 18 is V_8 and the base of T_2 is V_{out} of Figure 16. The actual zero offset condition from Figure 16 is

$$V_8 \approx V_{eb11} - \frac{1}{2} V_{R_{22}} - V_{Z2} - V_{eb8} \approx -4 \text{ v}$$

This simply amounts to decreasing the magnitude of the constant-current source, T_1, of Figure 18. With Y = +10 volts = X the inequalities above do not hold unless V is level-shifted down by four volts.

When this is done the conditions on Figure 18 become:

$$\frac{-X - 4}{G} \leq V \leq \frac{X - 4}{G} \tag{5.30a}$$

$$Z > X - \frac{G_0}{G} 4 \tag{5.37a}$$

$$i_1 = \frac{Z - 4}{R_4 G_0} \tag{5.40a}$$

$$\frac{R_6}{R_4 + R_5} [\frac{X}{G_0} + 4f + \frac{Z}{G_0}] < \text{minimum of } [Y - X + 4, \frac{R_6(Z - 4)}{R_4 G_0}] \tag{5.41a}$$

$$(X + Z + 4f G_0) < (Z - 4)(1 + \frac{R_5}{R_4}) \tag{5.43a}$$

$$(X + Z + 4f G_0) \frac{R_7}{R_8} < Y - X + 4 \tag{5.46a}$$

A similar analysis performed on a PNP two-stage amplifier produces similar equations. The values chosen satisfy these inequalities.

5.10 V_{eb} Variations and Gain

No attempt will be made in this section to consider the effects of changes in parameters other than V_{eb}. The analysis of the input stage in Section 5.4 and of the second stage in Section 5.5 considered all major variations in the transistor parameters.

The overall effect of the V_{eb} variations on the gain will now be presented. Only V_{eb} variations due to current level changes will be considered. Thermal variations in V_{eb} will be discussed in Section 5.13. Following this discussion of the effect of V_{eb} variations on gain, the effect of these variations on the linearity of the amplifier will be presented.

The circuit of Figure 16 is used for this analysis. α is assumed to be one. This is a quite valid assumption if all transistors have a $\beta > 50$. The current in T_n will be designated i_n. The constant currents I_5 and I_6 will be designated by capital letters. The $|V_{eb}|$ of transistor T_n will be designated V_{ebn}. The base of transistor T_n will be designated V_n. The bases of T_4 and T_2 will be designated V'_{out}. These conventions will apply in the remainder of this thesis.

By considerable algebraic manipulation, it can be shown that:

$$V_8 = \frac{R_9 R_5}{R_{10}} \left[\frac{I_5}{2} - \frac{V_{out} R_{20}}{(R_1 + R_2)(R_{20} + R_{21})} + \frac{V_{eb2} - V_{eb1}}{R_1 + R_2} + \frac{V_{in}}{R_1 + R_2}\right] - \frac{R_5}{R_{10}} V_{eb7} - 25 \tag{5.47}$$

$$V_9 = 25 - \frac{R_{12} R_8}{R_{11}} \left[\frac{I_6}{2} + \frac{V_{out} R_{20}}{(R_3 + R_4)(R_{20} + R_{21})} - \frac{V_{in}}{R_3 + R_4} + \frac{V_{eb4} - V_{eb3}}{R_3 + R_4}\right] + \frac{R_8}{R_{11}} V_{eb10} \tag{5.48}$$

As V_{in} increases, V'_{out} increases, but the increase in V_{in} is greater than the increase in V'_{out}. Similarly, as V_{in} decreases, V'_{out} decreases and the decrease in V_{in} is larger than the decrease in V'_{out}.

For a positive input voltage increment i_1, i_7, V_8, and V_9 increase and i_3 and i_{10} decrease. For a negative voltage increment i_1, i_7, V_8, and V_9 decrease and i_3 and i_{10} increase.

Equation (5.47) is rewritten designating in parenthesis after V_{eb} the current to which V_{eb} is directly proportional,

$$V_8 = \frac{R_9 R_5}{R_{10}} \left[\frac{I_5}{2} - \frac{V'_{out}}{2R_1} + \frac{V_{in}}{2R_1} + \frac{V_{eb2}(-i_1) - V_{eb1}(i_1)}{2R_1}\right]$$

$$- \frac{R_5}{R_{10}} V_{eb7}(i_7) - 25 \quad . \tag{5.49}$$

Defining ∂V_n as the change in V_n for a given change in V_{in}, equation (5.49) becomes

$$\partial V_8 = \frac{R_5 R_9}{2R_1 R_{10}} [\partial V_{in} - \partial V'_{out} + \partial V_{eb2}(-i_1) - \partial V_{eb1}(i_1)]$$

$$- \frac{R_5}{R_{10}} \partial V_{eb7}(i_7) \quad . \tag{5.50}$$

Using the specified resistor values ∂V_8 becomes

$$\partial V_8 = 107[\partial V_{in} - \partial V'_{out} + \partial V_{eb2}(-i_1) - \partial V_{eb1}(i_1)] - 10\partial V_{eb7}(i_7) \tag{5.51}$$

For the case of $\partial V_{in} > 0$,

$$\begin{aligned} \partial V_{eb1} &> 0 \\ \partial V_{eb2} &< 0 \\ \partial V_{eb7} &> 0 \\ \partial V'_{out} &> 0 \end{aligned} \tag{5.52}$$

$$\partial V_9 = 107 [\partial V_{in} - \partial V'_{out} - A] - 10B \quad . \tag{5.53}$$

where

$$A = -\partial V_{eb2} + \partial V_{eb1}$$

and

$$B = \partial V_{eb7}$$

are positive numbers since by equation (5.52)

$$\begin{aligned} -\partial V_{eb2} &> 0 \\ +\partial V_{eb1} &> 0 \\ +\partial V_{eb7} &> 0 \quad . \end{aligned}$$

Thus as V_{in} increases V_8 increases but the increase is reduced by the ∂V_{eb} values. For the case of $\partial V_{in} < 0$,

$$\begin{aligned} \partial V_{eb1} &< 0 \\ \partial V_{eb2} &> 0 \\ \partial V_{eb7} &< 0 \\ \partial V'_{out} &< 0 \end{aligned} \tag{5.54}$$

$$\partial V_8 = 107[\partial V_{in} - \partial V'_{out} + C] + 10D \tag{5.55}$$

where

$$C = \partial V_{eb2} - \partial V_{eb1} > 0$$

$$D = -\partial V_{eb7} > 0$$

since by equation (5.54)

$$\begin{aligned} \partial V_{eb2} &> 0 \\ -\partial V_{eb7} &> 0 \\ -\partial V_{eb1} &> 0 \quad . \end{aligned}$$

As V_{in} decreases V_8 decreases but the effect of the V_{eb} variations will be to reduce the decrease.

The conclusion from these two cases is that the effect of the V_{eb} parameters on the circuit will be to reduce the gain at V_8 below its theoretical value which assumes V_{eb} = constant.

If a similar analysis is carried out for V_9, a similar result will be obtained. The effect of V_{eb} variations will thus tend to reduce the overall amplification of the circuit slightly below its theoretical value.

5.11 V_{eb} Variations and Linearity

Such variations in V_{eb} will make the amplification of the circuit difficult to predict although it is ultralinear. But it is not necessary that the gain be within 0.5 per cent of a specified value since the potentiometer settings in the voltage dividers of Figure 8 can be adjusted according to the value of the gain. The important point is that the gain be extremely constant.

Before investigating the effect of V_{eb} variations on linearity, the various current levels in the circuit will be determined. It is easily verified that the approximate current levels are as shown in Table 1. The equations for ∂V_8 and ∂V_9 are

$$\partial V_8 = 107[\partial V_{in} - \partial V'_{out} + \partial V_{eb2}(-i_1) - \partial V_{eb1}(i_1)] - 10\partial V_{eb7}(i_7) \tag{5.56}$$

$$\partial V_9 = 107[\partial V_{in} - \partial V'_{out} + \partial V_{eb3}(i_2) - \partial V_{eb4}(-i_2)] + 10\partial V_{eb10}(i_{10}) \quad . \tag{5.57}$$

Table 1. Current Levels for $-10 \leq V_{out} \leq +10$ volts.

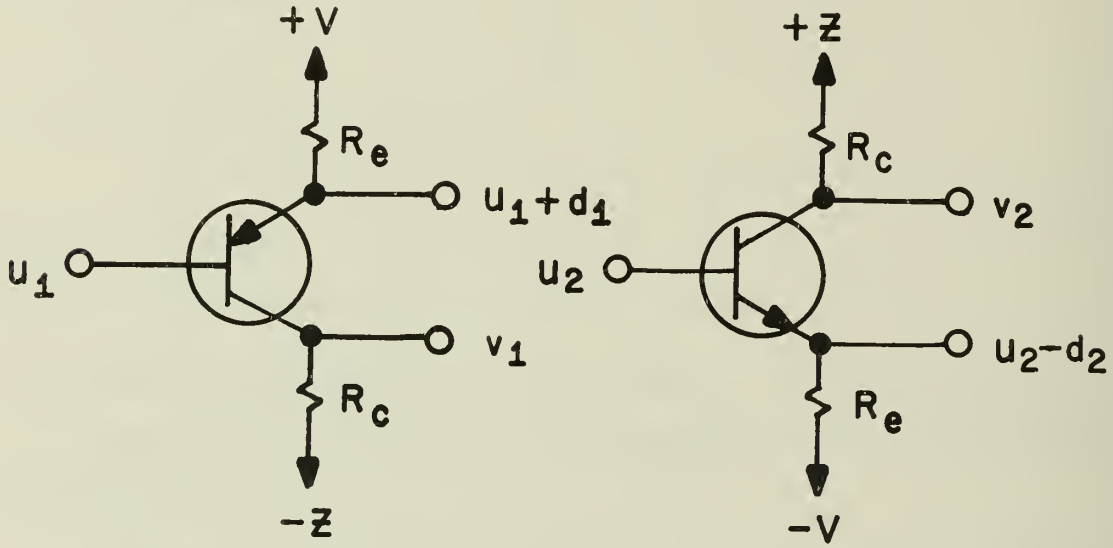
Current	min. - ma	max. - ma
i_1	.25	.68
i_2	.32	.75
i_3	.25	.68
i_4	.20	.63
i_5	.955	.955
i_6	.88	.88
i_7	1.08	3.08
i_8	10	10
i_9	10	10
i_{10}	1.08	3.08

The variation in current in the input stage is quite small as is the current level. This portion of the V_{eb} versus i_c curve should have a rather linear variation in V_{eb} and positive increments in V_{eb} should be nearly the same as negative increments for equal and opposite i_c increments. The V_{eb} variations in the difference amplifier stage were seen not to cancel, as the two V_{eb} values do, but to add. Due to the low current levels, the V_{eb} variations will be quite linear. Since the total current in both transistors is constant the entire first stage variation will be very linear. The variation in V_{eb} in the second stage transistors should be about the same as in the first stage since the current range is wider but the values are higher thus reducing the slope of the V_{eb} versus I_c curve. These portions of the V_{eb} versus I_c curve can be linearized and treated as straight lines such that equal and opposite increments of current produce equal and opposite changes in V_{eb}.

These variations in V_{eb} will thus be quite linear and the voltages at V_8 and V_9 should increase linearly; thus, the gain remains rather constant even though V_{eb} varies and its variation is multiplied by the gains of the various stages.

5.12 Influence of Thermal Variations

Figures 19a and 19b show a PNP and a NPN transistor amplifier corresponding to T_7 and T_{10}, the second stage amplifiers of Figure 16.



(a) PNP (b) NPN

Figure 19. Transistor Amplifier Stages.

The power dissipation for the PNP amplifier is determined as follows:

$$i_e = \frac{V - u_1 - d_1}{R_e}$$

$$v_1 = -Z + R_c i_c = -V_Z + \alpha \frac{R_c}{R_e} (V - u_1 - d_1)$$

$$P_{c1} = (u_1 + d_1 - v_1)\, i_c$$

$$P_{c1} = \frac{\alpha}{R_e}\,[V - (u_1 + d_1)][Z - \alpha \frac{R_c}{R_e} v_1 + (1 + \alpha \frac{R_c}{R_e})(u_1 + d_1)]$$

where

$$d_1 = V_{eb7}\,.$$

The power dissipation for the NPN amplifier is similarly determined as follows:

$$i_e = \frac{u_2 - d_2 + V}{R_e}$$

$$v_2 = Z - R_c i_c = Z - \alpha \frac{R_c}{R_e} (u_2 - d_2 + V)$$

$$P_{c2} = (-u_2 + d_2 + v_2)\, i_c$$

$$P_{c2} = [\, -u_2 + d_2 + Z - a \frac{R_c}{R_e} (u_2 - d_2 + V)] \frac{\alpha}{R_e} (u_2 - d_2 + V).$$

where

$$d_2 = V_{be10}\,.$$

Denoting $\alpha \frac{R_c}{R_e} = g$ = gain of the amplifier stage, the power dissipation can be plotted as in Figure 20a and 20b. The actual values are listed below the graph and the initial value of $u_2 - d_2$ and $u_1 + d_1$ is shown (u at $V_{in} = V_{out} = 0$).

The voltages $u_1 + d_1$ and $u_2 - d_2$ vary by about ± 0.8 volts from their initial value for an output voltage range of $+8 \leq V_{out} \leq -8$ volts. Over this range of operation the P_c versus u curves can be linearized and approximated as straight lines.

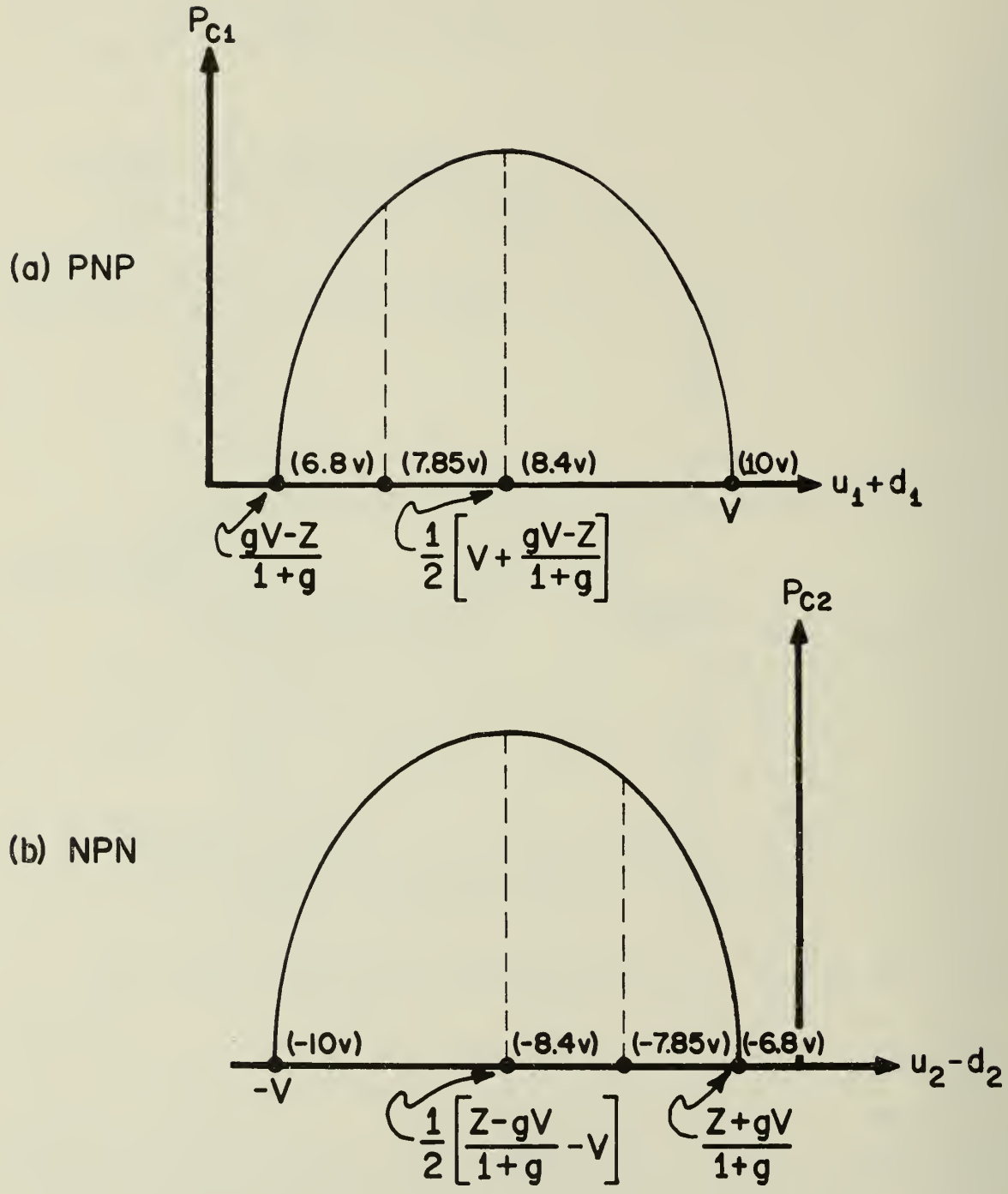


Figure 20. Power Dissipation for the Transistor Amplifier Stages of Figure 19(a,b).

An V_{in} increases both u_1 and u_2 decrease, and as V_{in} decreases both u_1 and u_2 increase. Also, due to the circuit topology u_1 and u_2 always change by equal amounts and in the same directions. As $u_1 + d_1$ increases P_{c1} increases, but as $u_2 - d_2$ increases P_{c2} decreases and vice versa. Since these portions of the power dissipation curves have been linearized the increases in P_{c1} equal the corresponding decreases in P_{c2}.

Thus

$$\partial u_1 = \partial u_2$$

$$\partial P_{c1} = \partial P_{c2} \quad .$$

A similar analysis performed on both first stages yields the following results:

$$\partial i_3 = \partial i_2$$

$$\partial i_1 = \partial i_4$$

$$\partial P_{c1} = \partial P_{c4}$$

$$\partial P_{c3} = \partial P_{c2} = -\partial P_{c1} = -\partial P_{c4} \quad .$$

As power dissipation increases, junction temperature increases, the increase being determined by the thermal resistance of the semiconductor.

$$\Delta T = \theta \Delta P_c$$

It can be shown that as temperature increases V_{eb} decreases. The emitter current is proportional to the minority carrier density just inside the base since the forward current across a PN junction is largely holes. This forward current is approximately proportional to this minority carrier density divided by the base width. If the emitter current is to remain unchanged for two temperatures T_1 and T_2, the hole density must remain constant as temperature varies. Defining p_{bn} as the minority carrier density just inside the base at temperature T_n, it follows that:

$$p_{b1} \exp. \left(\frac{qV_1}{kT_1}\right) = p_{b2} \exp. \left(\frac{qV_2}{kT_2}\right)$$

$$\frac{p_{b1}}{p_{b2}} = \exp.\left[\frac{q}{k}\left(\frac{V_2}{T_2} - \frac{V_1}{T_1}\right)\right] \simeq \frac{n_{i1}^2}{n_{i2}^2}$$

$$\frac{p_{b1}}{p_{o2}} = \exp.\left[-q\,\frac{E_g}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

$$\frac{E_g - V_2}{T_2} = \frac{E_g - V_1}{T_1} \quad .$$

For $E_g \gg V_1, V_2$

$$\frac{T_2}{T_1} = \left(1 + \frac{\Delta T}{T_1}\right) = \frac{1 - \frac{V_2}{E_g}}{1 - \frac{V_1}{E_g}} \simeq 1 + \frac{V_1}{E_g} - \frac{V_2}{E_g} \quad .$$

Thus

$$\frac{\Delta T}{T_1} \simeq - \frac{\Delta V}{E_g}, \quad \Delta V = - \left(\frac{\Delta T}{T_1}\right) E_g$$

It has been found experimentally that, for Germanium and Silicon transistors, for currents in the ma range, V_{eb} decreases by about 2.5 mv for each degree centigrade increase in temperature.

Hereafter P_n will denote the collector power dissipation of transistor n and T_n' will denote the junction temperature of transistor n.

5.13 Effect of Thermal V_{eb} Variations

As V_{in} increases P_2, P_3, and P_7 decrease and P_1, P_4, and P_{10} increase; thus T'_2, T'_3, and T'_7 decrease and T'_1, T'_4, and T'_{10} increase; thus V_{eb2}, V_{eb3}, and V_{eb7} increase; and V_{eb1}, and V_{eb10} decrease. Similarly as V_{in} decreases P_2, P_3, and P_7 increase and P_1, P_4, and P_{10} decrease; thus T'_2, T'_3, and T'_7 increase and T'_1, T'_4, and T'_{10} decrease; thus V_{eb2}, V_{eb3}, and V_{eb7} decrease and V_{eb1}, V_{eb4}, and V_{eb10} increase.

By equations (5.56) and (5.57) these thermal V_{eb} variations are observed to cancel since

$$\partial V_{eb7} = -\partial V_{eb10}$$

$$\partial V_{eb1} = \partial V_{eb4} = -\partial V_{eb2} = -\partial V_{eb3} \quad .$$

Similar results are observed if V_{in} decreases.

This tends to produce a circuit which is not affected by temperature variations over the desired output range.

5.14 Output Stage Compensation

The analyses of the previous sections have produced the following results:

(1) Parameter variations due to current levels will tend to decrease the gain at V_8 and V_9, and these variations will be approximately linear. Thus, V_8 will tend to vary by the same amount and in the same direction as V_9.

(2) Thermal variations due to temperature tend to cancel at V_8 and V_9.

Obviously the linear approximations used are not exact and the variations at V_8 and V_9 will not be exactly linear or drift-free. The

constant-current output stage will further compensate for any deviations present at V_8 and V_9.

By defining $\partial(V_9 - V_8)$ as the deviation in $(V_9 - V_8)$ from its initial value at $V_{in} = V_{out} = 0$, the effect of the output stage may more easily be discussed.

If $\partial(V_9 - V_8) > 0$, implying that V_9 has increased by more than V_8, a large output current would be expected and V_{out} would be too large. This does happen actually but the error is drastically reduced.

For

$$\partial(V_9 - V_8) > 0 \ ,$$

$$V_9 - V_8 = V_{eb9} + V_{Z1} + V_{R_{22}} + V_{Z2} + V_{eb8} \ ,$$

the modified output stage current increases. Thus,

$$\partial V_{eb9} > 0$$
$$\partial V_{eb8} > 0$$
$$\partial V_{Z1} > 0$$
$$\partial V_{Z2} > 0$$

which implies

$$\partial(V_9 - V_8) - (\partial V_{eb9} + \partial V_{Z1} + \partial V_{Z2} + \partial V_{eb8}) = \partial V_{R_{22}} \ .$$

The change in V_{eb} and V_Z is about the same and for

$$\partial(V_9 - V_8) \approx .3 \text{ v} \ , \ \partial V_{eb} \approx \partial V_Z \approx 50 \text{ mv} \ .$$

Therefore $\partial V_{R_{22}} \approx 0.1$ v, which shows that much of the nonlinearity has been accounted for by V_{eb8}, V_{eb9}, V_{Z1}, and V_{Z2} variations. The variation, $\partial V_{R_{22}}$, is reduced further by the fact that $\partial V_{11} = K\partial V_{R_{22}}$ where K is approximately 0.5. Thus in the experimental values above, $\partial V_{11} \approx 0.05$ volts.

Thermal variations are similarly reduced at V_{11} by a factor of about one-fourth.

The gain of a single two-stage amplifier as used in Figure 16 has been found to be constant within two per cent for Germanium and 2.7 per cent for Silicon transistors. The error of the amplifier of Figure 16 is 0.33 per cent. This is one-sixth of the error of a single two-stage amplifier. This factor of one-sixth is the same as appeared above in the experiment involving variations in the modified constant-current output stage parameters.

As V_9 increases, V_8 increases, thus P_{c9} decreases, and P_{c8} increases, or vice versa. It is easily shown that

$$\partial P_9 = -\partial P_8$$

since emitter currents are constant. Thus,

$$\partial T_9 = -\partial T_8.$$

From which

$$\partial V_{eb9} = -\partial V_{eb8}$$

Thus the temperature changes in T_8 and T_9 are such that they tend to maintain the output voltage at its proper value and the modified output-stage current constant.

Similarly, the output stage reduces any thermal drift present at V_8 and V_9 by a factor of about one-fourth. Its effect in reducing linearity variations at V_9 and V_8 is considerably higher, the factor being about one-sixth.

Due to the effect that T_7 and T_{10} have in reducing thermal drift and improving the linearity of the gain and the effect that T_9 and T_8 have in further reducing these errors, T_7 and T_{10} and T_8 and T_9 will be designated circuit-compensating transistor pairs since their compensating ability is due to their position in the circuit and not to a match of transistor parameters.

5.15 Experimental Data

Table 2 contains experimental data on the voltage amplifier of Figure 16. A digital voltmeter, accurate to within 2 mv was used for these measurements. The fact that the digital voltmeter had this error made it necessary to step down a high input voltage in order that readings accurate to below 1 mv could be obtained. An error of 2 mv in the reading of an input voltage would be magnified by 21 and the output voltage would be accurate only to within 42 mv. This is approximately twice the error of the voltage amplifier.

For these reasons the input column is headed V'_{in}. Column three shows the increments in V_{out} for equal increments in V_{in}. All of the output increments are accurate to within 0.8 per cent of the average value, the largest difference being 28 mv. Column four shows the gain of the amplifier calculated to four figures. The gain is seen to be extremely linear, the largest deviation from the value G = 21.38 is 0.33 per cent. Column five shows the deviation in output voltage caused by a load requiring 10 ma at all voltages. The largest error due to loading was observed to be a 15 mv decrease in output voltage.

Table 2. Test Data.

V'_{in} (volts)	V_{out} (volts)	ΔV_{out} (mv)	Gain	V_{out} Loaded (mv)
0.000	0.000			-8
+1.000	+1.020	1020	21.42	-8
+2.000	+2.036	1016	21.38	-10
+3.000	+3.060	1024	21.42	-10
+4.000	+4.064	1004	21.34	-10
+5.000	+5.086	1022	21.36	-12
+6.000	+6.100	1014	21.36	-12
+7.000	+7.120	1020	21.36	-12
+8.000	+8.135	1015	21.36	-14
+9.000	+9.166	1031	21.38	-15
0.000	+0.008			
-1.000	-1.015	1015	21.32	-9
-2.000	-2.039	1024	21.41	-8
-3.000	-3.050	1011	21.35	-9
-4.000	-4.082	1032	21.42	-9
-5.000	-5.100	1018	21.42	-8
-6.000	-6.125	1025	21.44	-8
-7.000	-7.140	1015	21.42	-8
-8.000	-8.160	1020	21.42	-8
-9.000	-9.166	1006	21.38	-8

The largest output offset voltage (V_{out} when $V_{in} = 0$) was observed when the input was kept at its maximum or minimun value for a while and then grounded. The maximum such offset voltage observed was 8 mv.

The largest drift was observed at the higher voltages when the input was kept at its maximum or minimum level and then the polarity reversed. The largest such drift observed was 8 mv.

5.16 Component Replacement

The resistor values have been chosen so that the potential difference across R_{22} in Figure 16 is 1.0 volts with the high side being +0.6 volts and the low side being -0.4 volts. These values assume a V_{eb} of 0.14 volts for Germanium and 0.78 volts for Silicon transistors (T_8, T_9). The value 1.0 volts is not critical; it is only necessary that the voltage be in the neighborhood of 1.0 volts and that the value about 0.14 volts be somewhere within the 1 volt range at $V_{in} = 0$ for zero offset. The collector resistors R_6 and R_7 place an upper limit on the collector current and on the voltage across the potentiometer. This upper limit is found from

$$V_{Z1} + V_{Z2} + I_c + 2V_{eb} + 2V_{cb} = 2(50 - I_c) \tag{5.58}$$

Assuming

$$\begin{aligned} V_{eb} &= .78 \text{ v for Silicon Transistors} \\ V_{cb\ min} &= 1 \text{ v for Silicon Transistors} \\ V_{Z1} &= V_{Z2} = 2.9 \text{ v} \end{aligned} \tag{5.59}$$

The maximum collector current is

$$I_c \approx 19 \text{ ma} \tag{5.60}$$

This voltage increment of 1.0 volts will vary somewhat as transistors are interchanged but this voltage difference was found sufficient to account for most V_{eb} and β variations between transistors. Naturally, to keep the circuit values as given, Germanium transistors must be replaced only by Germanium units, and similarly for Silicon transistors.

New resistor values could be calculated if it was desired that all of the transistors be Germanium or Silicon. The only two resistors that would have to be changed would be R_{16} and R_{19} which determine the magnitude of the constant-current source and sink.

The V_{eb} versus I_c curve for Germanium is rather linear and the knee is not very pronounced. For this reason it is quite easy to find replacements for Germanium units since for almost all Germanium transistors the $I_c = 0.5$ ma point is situated such that the curve of V_{eb} versus I_c can be quite easily linearized in the used region surrounding this operating point.

The knee of the V_{eb} versus I_c curve for Silicon is more pronounced than in Germanium units and its position is not nearly the same between two different NPN or PNP types. In general it has been observed on a curve-tracer that the knee occurs at values as low as $I_c = 0.1$ or 0.2 ma in Silicon PNP units and as high as $I_c = 0.8$ ma in many Silicon NPN units. For this reason when using this amplifier with all Silicon transistors more care must be given to the choice of current levels in the input difference amplifiers. If nonlinearities are observed at the output, data can be taken for ∂V_7 and ∂V_{10} for $V_{in} = \pm 0.2$ volts, $V_{in} = \pm 0.3$ volts, and $V_{in} = \pm 0.4$ volts. It has been found that ∂V_7 or ∂V_{10} will be constant for either positive or negative increments in ∂V_{in} and not constant for the opposite signed increments. This information will tell whether the I_c operating point is sufficiently above or below the knee of

the V_{eb} curve to use a linear approximation or whether the operating point is too close to the knee of the curve, thus indicating an increase or decrease in the operating point current, I_c.

For the two Silicon transistors SM5306(NPN) and 2N3638(PNP), the following values were changed to increase the current in the PNP difference amplifier by a factor of four. This was necessary since the knee of the V_{eb} curve for the 2N3638 occurs at about 0.5 ma.

$R_{19} = 4.65$ K Ω $\quad$ $R_{12} = 1.3$ K Ω

$R_{18} = 10\ \Omega$ $\quad$ $R_{14} = 15$ K Ω

$R_{17} = 4$ K Ω $\quad$ $R_{15} = 10$ K Ω

$R_3 = R_4 = 62\ \Omega$ $\quad$ $R_{16} = 2.7$ K Ω

All other values are as before.

It is much easier to obtain an operating current on the V_{eb} versus I_c curve where the useable portion of the curve may be linearized by increasing the currents. Care should be used in increasing these input stage currents since the thermal drift increases by about the same factor by which the first stage currents are increased. This follows from equations (5.56) and (5.57) and a consideration of the magnitudes of $\Delta P_{c\ \text{first stage}}$ and $\Delta P_{c\ \text{second stage}}$. $\Delta P_{c\ \text{first stage}}$ will be increased by approximately the factor by which the input stage currents are increased. If the second stage currents are not changed the thermal variations in the second stage is not sufficient to cancel the thermal variation of the first stage. The 10 K Ω and 1 K Ω resistors in the second stage could be decreased by twice the factor by which the first stage currents were increase thus increasing $\Delta P_{c\ \text{second stage}}$, enabling the second stage thermal drift to be of sufficient magnitude to cancel the first stage thermal drift. It is thus much better, if the magnitude of I_c at the V_{eb} knee allows, to decrease the first stage currents and increase the first stage resistors to obtain linearity of operation without a corresponding increase in drift.

5.17 Output Range

An output range of $-10 \leq V_{out} \leq +10$ volts was desired. This is determined by the circuits which the voltage amplifier must drive. An output of $-12 < V_{out} < +12$ volts can be tolerated. The +10 volts collector supply of T_{11} insures the upper limit on V_{out}. To determine the lower limit on V_{out} the critical voltages and currents at which the various transistors cut-off is investigated.

Transistor T_1

$$i_1 = \frac{i_5}{2} + \frac{V_{in} - V_{out}}{2R_3} = .477 + .455\ V_{in} \qquad (5.61)$$

The maximum i_1,

$$i_{1\ max.} = .955\ ma = i_5, \qquad (5.62)$$

occurs at

$$V_{in} = 1.05\ v\ . \qquad (5.63)$$

The minimum i_1,

$$i_{1\ min.} = 0\ ma, \qquad (5.64)$$

occurs at

$$V_{in} = -1.05\ v\ . \qquad (5.65)$$

Transistor T_3

$$i_3 = \frac{i_6}{2} - \frac{V_{in} - V_{out}}{2R_3} = .44 - .455\ V_{in} \tag{5.66}$$

The maximum i_3,

$$i_{3\,max.} = 0.88 \text{ ma} = i_6 , \tag{5.67}$$

occurs at

$$V_{in} = -0.97 \text{ v} . \tag{5.68}$$

The minimum i_3,

$$i_{3\ min.} = 0 \text{ ma} , \tag{5.69}$$

occurs at

$$V_{in} = 0.97 \text{ v} . \tag{5.70}$$

As above, for any inputs outside of this range, the value of i_1 and i_3 remain at their maximum or minimum, the only limits being on the collector base junctions of the transistors.

Transistor T_7

The collector base junction of T_7 must also be properly biased, that is,

$$-25 + \frac{R_9 R_5}{R_{10}} i_1 - R_5 V_{eb7} < 10 - R_4 i_1 . \tag{5.71}$$

Assuming average V_{eb} values

$$i_1 < .686 \text{ ma}$$
$$V_{in} < .461 \text{ v} \quad . \tag{5.72}$$

Transistor T_{10}

The collector base junction of T_{10} must be properly biased, that is,

$$25 - \left(\frac{R_{12}\, i_3}{R_{11}} - V_{eb10}\right) R_8 > -10 + 4.7 i_3 \quad . \tag{5.73}$$

Assuming average V_{eb} values

$$i_3 < .655 \text{ ma}$$
$$V_{in} > -.475 \text{ v} \quad . \tag{5.74}$$

From the critical voltages and currents determined above, the lower limit on V_{out} can be calculated.

$V_{out\ min.}$ occurs at

$$V_{in} \approx -.475 \text{ v} \quad . \tag{5.75}$$

At this input value

$$i_3 = .655 \text{ ma}$$
$$i_1 = .22 \text{ ma} \quad . \tag{5.76}$$

Thus,

$$V_9 = -7.4 \text{ v} \tag{5.77}$$

$$V_8 = -16.2 \text{ v} \tag{5.78}$$

$$V_{R_{22}} = -7.4 - V_{eb9} - V_{Z1} - (-16.2 + V_{eb8} + V_{Z2}) = -11.2 - (-12.4) \tag{5.79}$$

$$= 1.2 \text{ v}$$

$$V_{out\ min.} \simeq -11.6 - V_{eb11} \tag{5.80}$$

$$V_{out\ max.} \simeq -11.75 \text{ v} \quad . \tag{5.81}$$

The experimentally measured value is

$$V_{out\ min.} = -11.5 \text{ v} \quad . \tag{5.82}$$

This is within the tolerable range and is acceptable. The originally desired range could be obtained by inserting a diode from the base of T_{11} to the -10 volts supply. This is not necessary in this application however.

The zener diodes Z1 and Z2 are necessary to obtain an output range of at least $-10 \leq V_{out} \leq +10$ volts due to the +10 and -10 volts supplies on T_7 and T_{10}. These supply voltages limit the maximum and minimum values of V_8 and V_9. The range of V_8 and V_9 could easily be extended by replacing the +10 and -10 volts supplies by +25 and -25 volts. This however requires that T_7 and T_{10} be chosen such that the collector-to-base breakdown voltage is at least 35 volts. This transistor specification is avoided by inserting Z1 and Z2 to step down the range of V_8 to $-14.2 \leq V_8 \leq +5.8$ volts and to step up the range of V_9 to $-5.8 \leq V_9 \leq +14.2$ volts, thus enabling T_7 and T_{10} to remain conducting throughout the desired output range.

5.18 Input Range

There are certain limits on the input voltage since for $V_{in} \geq 0.97$ volts the base of T_{10} is at -10 volts and for $V_{in} \leq -1.05$ volts the base of T_7 is at +10 volts. Thus the allowed input range is about

$$-9 < V_{in} < +9 \text{ v} \tag{5.83}$$

to insure the proper collector-to-base bias on T_1 and T_3.

The maximum value that V_{in} can have in its Paramatrix application occurs when a point on the edge of the matrix with coordinate voltage +8 volts is magnified by four and shifted right by 16 volts. Thus V_{in} can become

$$V_{in\ max.} = \frac{1}{G} [8m + a]$$

$$V_{in\ max.} \approx \frac{1}{20} (48) \tag{5.84}$$

$$V_{in\ max.} \approx 2.4 \text{ v} \quad .$$

The possible range of V_{in} is thus

$$-2.4 < V_{in} < +2.4 \text{ v} \quad . \tag{5.85}$$

Thus, there is no need for bumping diodes at the input to the voltage amplifier since the allowed range of equation (5.83) is not exceeded as shown by equation (5.85).

The input impedance of the voltage amplifier is essentially the parallel combination of the collector resistance of R_1 and R_2

$$Z_{in} \approx 600 \text{ K } \Omega$$

Since one input transistor is an NPN and the other a PNP, the base current at the input is less than it would be for a single two-stage

amplifier. This reduces any error due to current flowing into or from the summing point of the second stage voltage divider.

5.19 Frequency Range

The only limitation on the speed of operation appears to be the choice of transistors. The higher the alpha cut-off frequency of the transistors used, the better the frequency response. Fast zener diodes should also be used. With the transistors listed in Figure 16, the circuit performs satisfactorily with a 500 kc square-wave input with a rise time of 200 ns and a fall time of 100 ns. With Silicon SM5306 and 2N3638 transistors the circuit performs satisfactorily over 1 mc with rise times of 100 ns and fall times of 100 ns.

5.20 Single Two-Stage Amplifier Design

It is possible, although not practical due to component replacement difficulties to build one-half of the amplifier of Figure 16 with new values and with a loss of accuracy and an increase in drift.

A matched pair of very high β($\beta > 100$) transistors with almost identical characteristics, with β extremely constant and with very flat collector characteristics over the desired current range, can be selected on a curve-tracer for use in the input stage.

Similarly the collector characteristics for various loads can be plotted. A transistor with very good linearity over a wide current and voltage range and with a collector breakdown voltage greater than 35 volts can be selected for the second stage transistor.

Tests on the second stage transistor with the load used in plotting the collector characteristics can be tested to determine the best combination of gain and current levels that produce the most linear gain.

A similar test can be made on the first stage transistors to determine the best current levels for linearity with the stipulation that the product of the first stage gain and the second stage gain is greater than 100.

In this manner the single-stage amplifier of Figure 21 was designed. Its thermal drift is much worse than before, about 35 mv. Its offset has increased to about 25 mv and the gain is constant within one per cent.

5.21 Summary

This voltage amplifier has many advantages over other designs. It has excellent drift stability and very low offset values, both below 10 mv. Its output range is quite high for so accurate an amplifier. Its linearity is below 0.35 per cent. The compensation techniques used to achieve this unusually good stability are functions of the topology. The ease of replacement of components demonstrates how free this amplifier is from matched transistor pairs and various temperature compensating elements. Temperature compensating diodes and thermistors cannot actually be used due to the large voltage and temperature ranges since junctions which cool off at one output level may heat up at the next output value. The data of Table 2 was taken at d-c. When run at higher frequencies the performance actually increases since input levels are on for only very small fractions of seconds as opposed to fractions of minutes in a d-c test. Thus, the junctions will have much less time in which to heat up or cool down, reducing the parameter variations considerably.

There are certain disadvantages to this amplifier. It actually contains two voltage amplifiers and thus naturally has a rather large number of components and is not as simple an amplifier as is possible.

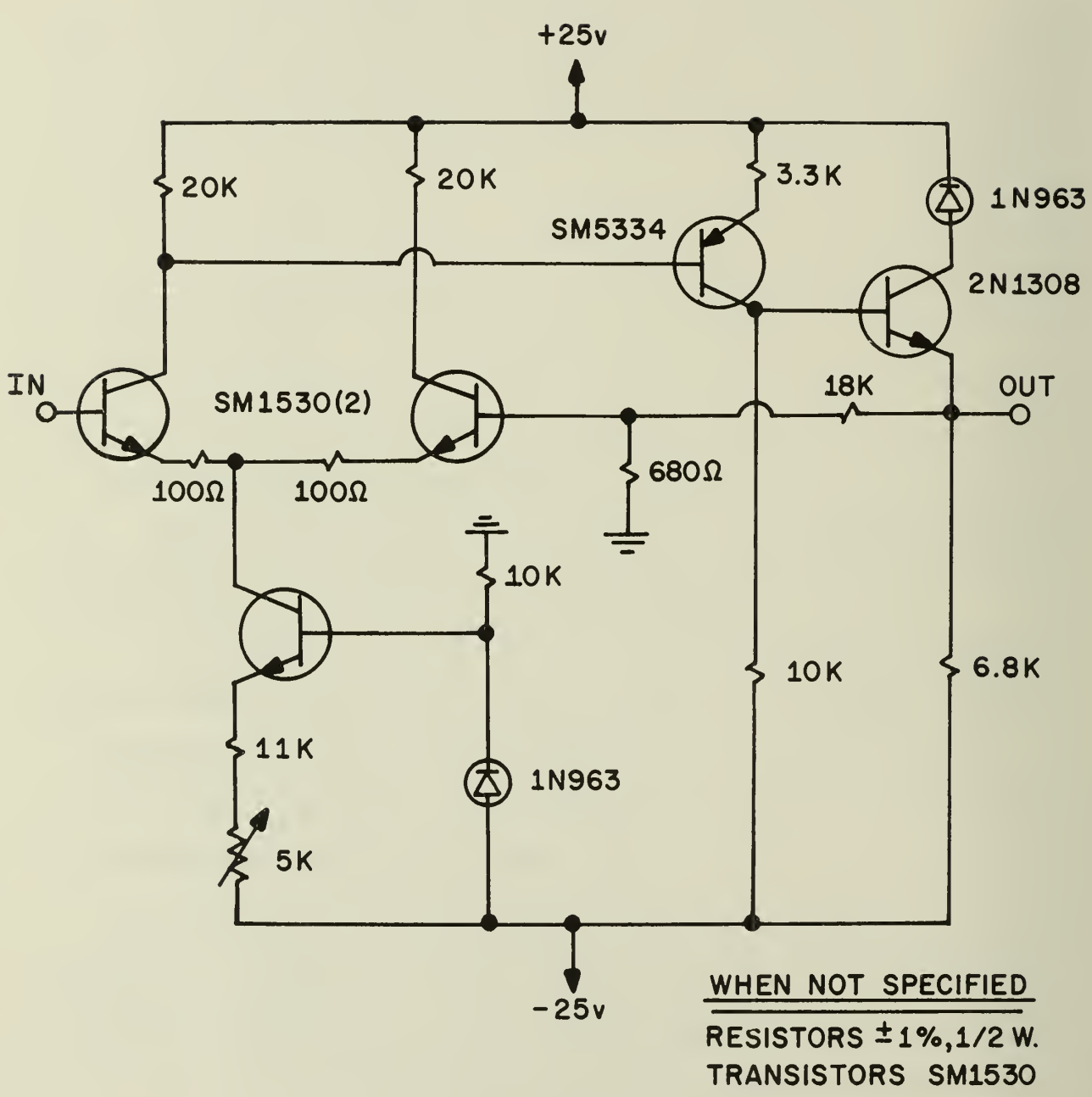


Figure 21. Single Two-Stage Amplifier.

This was found necessary since the drift and linearity compensation desired could not be obtained in a single two-stage amplifier.

A second disadvantage of this amplifier is that the gain which is so exact cannot be accurately predicted due to the number of components, the number of V_{eb} drops and other parameters which must be measured, and the unknown amount of variation which is not compensated for and which subtracts from the gain. The inconvenience of having to measure the gain on a meter and varying one of the feedback resistors until the desired gain is obtained is a small price to pay for the accuracy which such a configuration can produce. The number of components is still less than in many d-c amplifiers which have much less accuracy.

A diode could be placed in series with R_{18} and R_{15} for better temperature stability although it is not really necessary here since the power dissipation is rather constant in T_5 and T_6. Also a zener diode could be used in place of R_{18} and R_{15} for a more stable current source or sink. This again is not necessary since P_{c5} and P_{c6} are very constant.

6. CONCLUSION

This method of transforming line drawings which are displayed on a matrix of light bulbs has many interesting features.

1. It presents new applications for hybrid analog-digital circuit techniques.
2. It uses analog voltage levels to determine the matrix coordinates.
3. It employs diamond gates to gate analog signals by means of digital ones.
4. It sequentially scans the matrix by digital counters.
5. It contains a highly accurate current amplifier with unity voltage gain within 50 mv.
6. It involves an ultralinear, low drift, wideband voltage amplifier capable of amplification with an accuracy of 0.33 per cent over a wide output range.
7. It is capable of translating, rotating, and magnifying this line drawing at high speeds.

The desired accuracy of this system is one-half the voltage difference of adjoining coordinates or 250 mv. The accumulative worst-case error of the transformer from the sine-cosine potentiometer to the output of the voltage amplifier is approximately 230 mv which is within the desired accuracy.

Many of these circuits, notably the ultralinear voltage amplifier, have applications in many areas of engineering research. Various compensation techniques used in this amplifier have produced, over a wide voltage range, accuracies previously unattainable without the use of integrated circuit techniques or extensive chopper and rectifying circuits.

Amplifiers with very high accuracies are normally limited to frequencies below 100 kc. The minimum error of integrated circuit amplifiers is about one per cent and few of these had an output range of 20 volts. The amplifier described herein has an error of 0.33 per cent, a 20 volts output range, and can operate with a 1 mc square-wave input.

There are many possible applications for this ultralinear voltage amplifier. With a resistive summing network with a variable summing resistor, as an input circuit, the gain of the entire circuit can be varied from 1 to 20. If one input to the resistive summing network is connected to a variable power supply, the aforementioned variable gain is possible as well as a level-shifting of the output voltage.

Other obvious applications for such an amplifier involving different peripheral equipment are possible as the particular application warrants.

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13. ABSTRACT

By assigning analog voltages to the coordinates of a graph, drawings can be electrically displayed. By means of a sine-cosine potentiometer, resistance chains, and diamond gates with appropriate gate signals from digital counters, these drawings can be transformed (i.e., translated, rotated, magnified). Resistive summing networks and compensated current amplifiers provide the translation, while an ultralinear voltage amplifier achieves the magnification.

This ultralinear voltage amplifier consists essentially of two two-stage amplifiers feeding a constant-current pre-output stage with negative feedback applied to the first stages.

Thermal and nonthermal parameter variations are compensated for by a linearization of the used portions of the power dissipation and V_{eb} versus i_c curves, the constant-current output stage, and circuit compensating transistor pairs.

This topology produces an amplifier with a gain constant within 0.33 per cent, a 20 volt output range, a drift and offset voltage of less than 9 mv, and a frequency response of d-c to 1 mc with a square wave input. It can supply 10 ma at all voltage levels with an error of less than 16 mv. Component replacement is possible with no loss of accuracy.

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